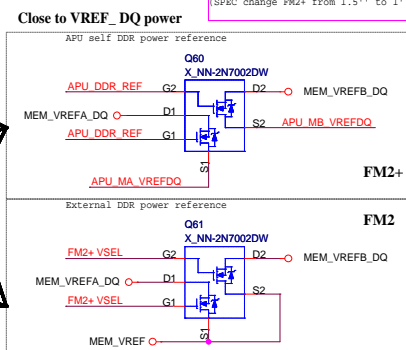
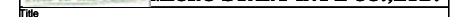


[illegible]

DEVICE	ADDRESS	CLOCK
DIMM 1	00	P/N_DDR1_A
DIMM 2	01	
DIMM 3	10	P/N_DDR1_B
DIMM 4	11	



FM2+ DDR3 I/F

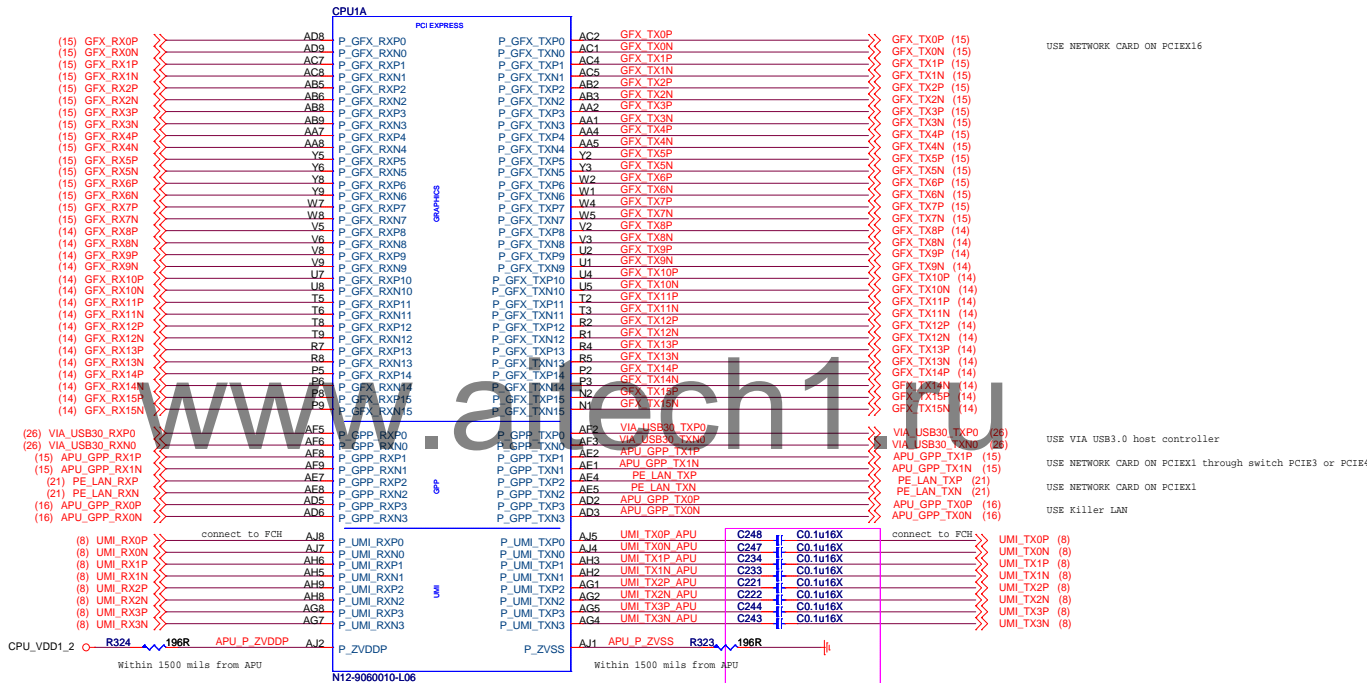
Size	Document Number	Rev
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Size	Document Number	Rev
Custom	MS-7000	1.0

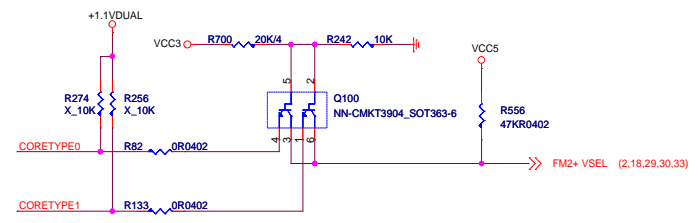
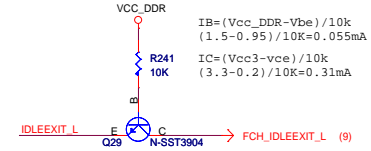
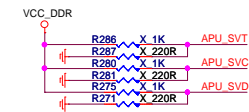
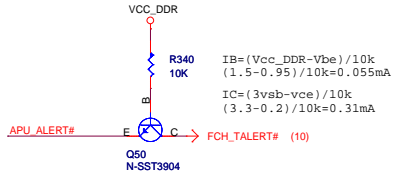
	MS-7900	1.0
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Date: Tuesday, December 10, 2013 Sheet 2 of 47

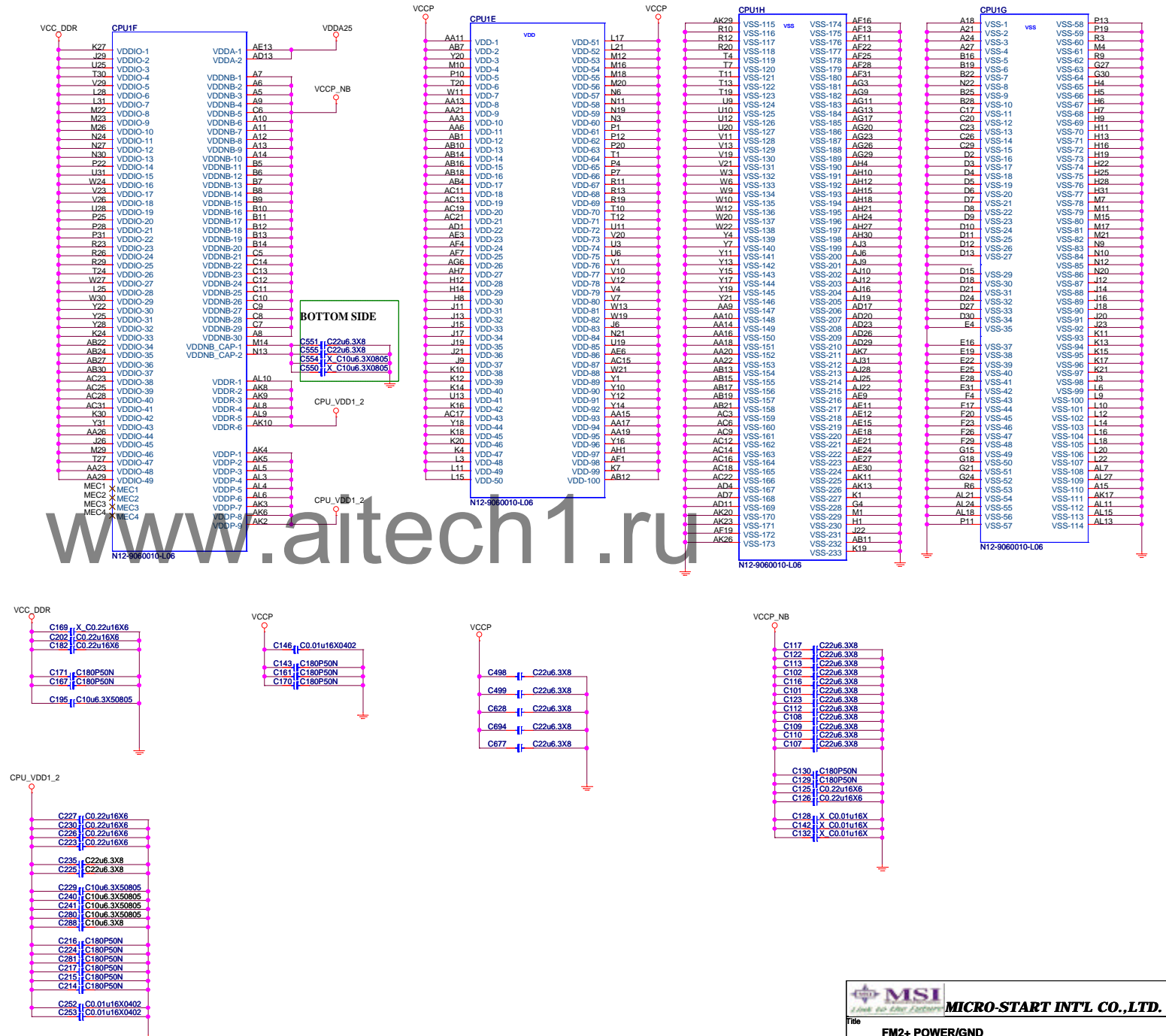
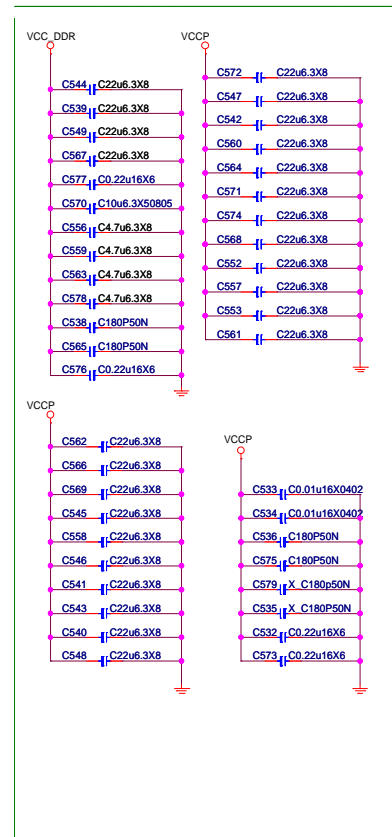
PCIE I/F

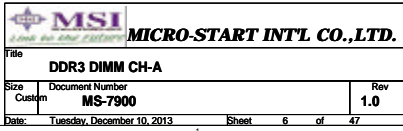


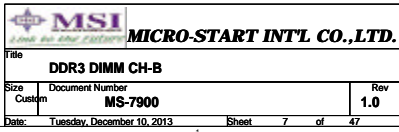
85ohm +/-10%
the CAP need over 500mil from the cpu PIN



BOTTOM SIDE







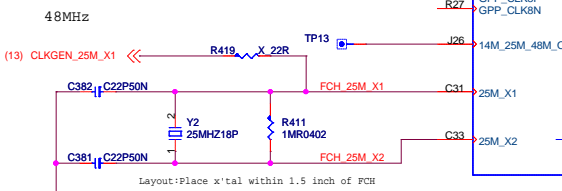
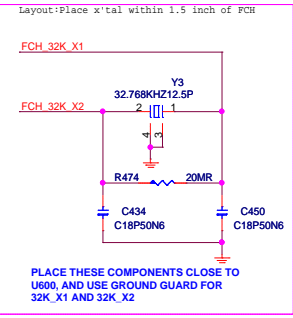
PCIE_RST#
X_C150p25N
A_RST#
X_C150p25N

A_RST# for LPC device:
PCIE_RST# for APU PCI device:

AC capacitor need
over 500mil
form the hudson

impedance 85ohm+/-15%
length need 1.0 to 12 inch

100MHz



HUDSON - D4

Part 1 of 5

PCIE_RST#

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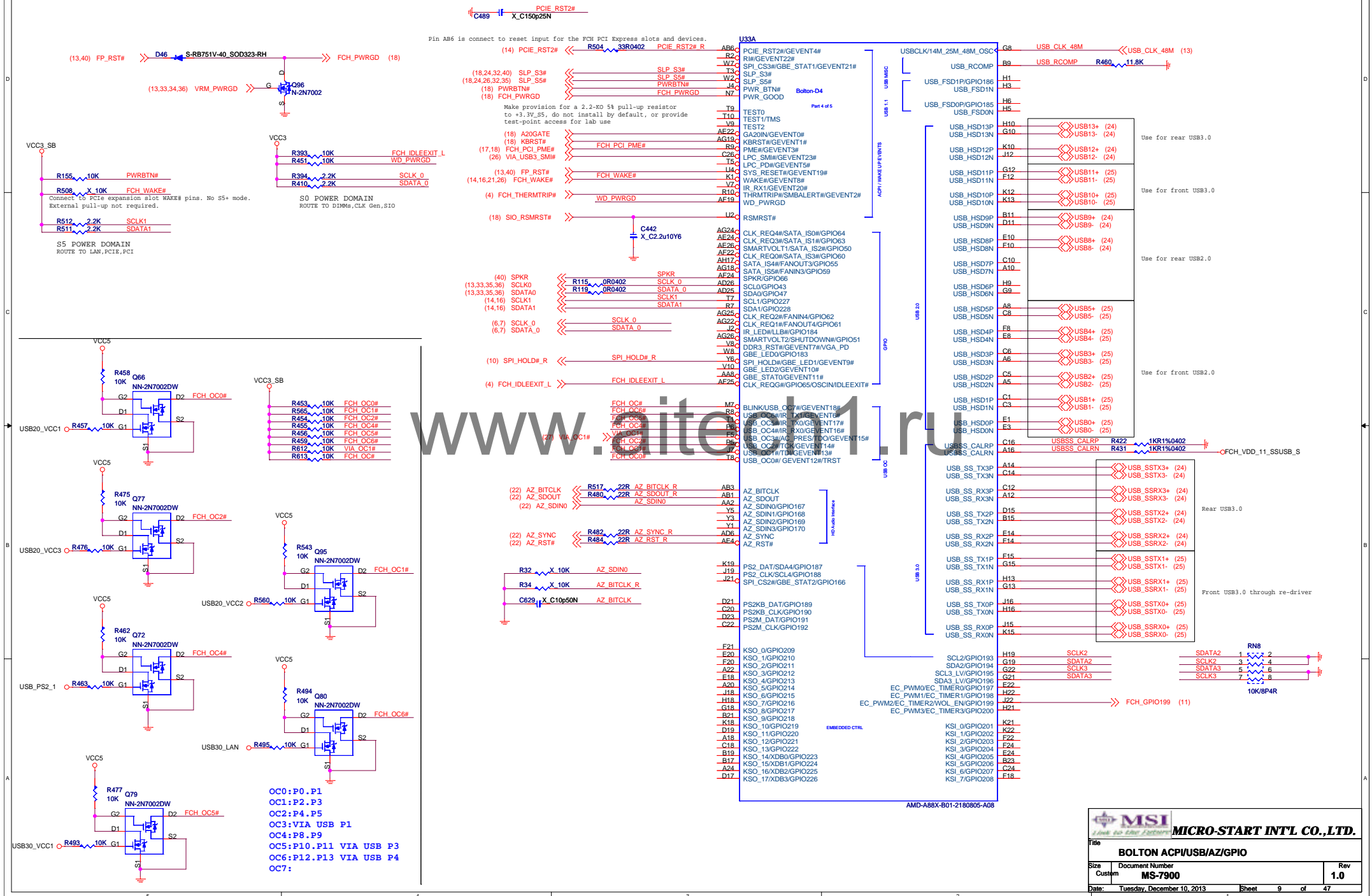
PCIE_RST#

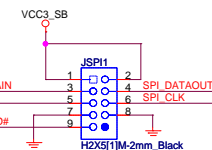
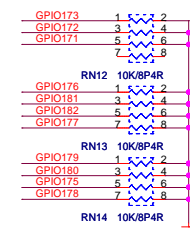
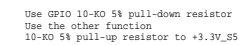
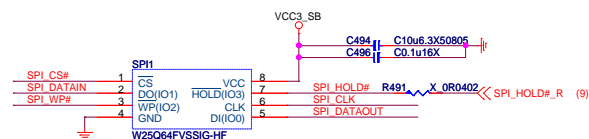
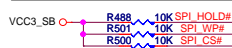
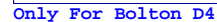
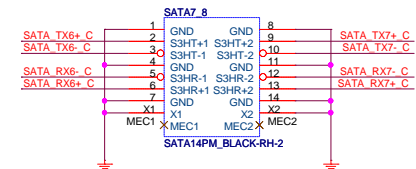
PCIE_RST#

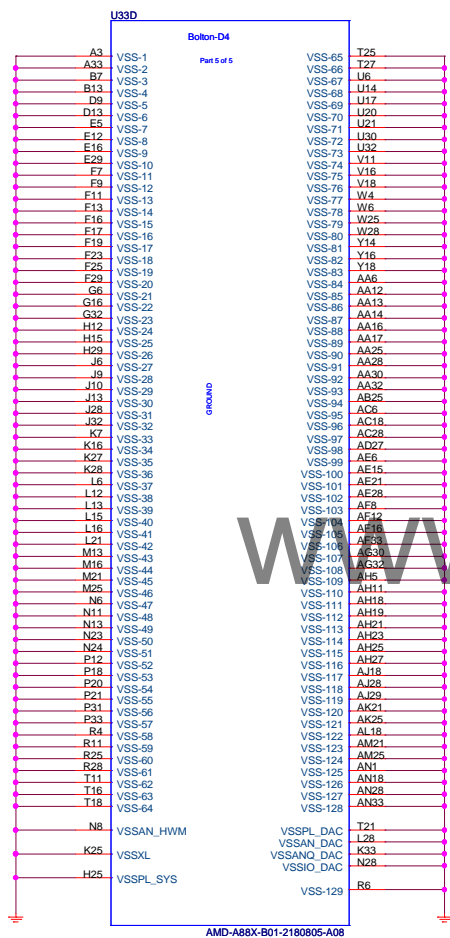
PCIE_RST#

PCIE_RST#

HUDSON ACPI/USB/AZ/GPIO

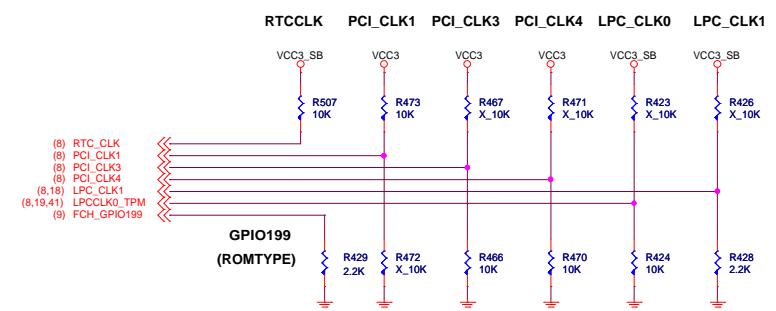






Layout:
VSSPL_SYS/VSSAN_HWM CONNECT TO GND
WITH A SEPRATED VIA

FCH REQUIRED STRAPS



	S5+ Mode RTCCLK	PCIeR GEN PCI_CLK1	Debug Strap PCI_CLK3	CLK GEN PCI_CLK4	IMC Enable LPC_CLK0	CLKGEN Enable LPC_CLK1	GPIO199 (ROMTYPE)
PULL HIGH	S5 Plus MODE DISABLED DEFAULT	PCIe interface at Gen2 DEFAULT	Enable Debug Straps	Reserved	EC ENABLED	CLKGEN ENABLED	LPC ROM
PULL LOW	S5 Plus MODE ENABLED	FORCE PCIe at Gen1	Disable Debug Straps DEFAULT	APU_CLK/DISP_CLK Required setting DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SPI ROM DEFAULT

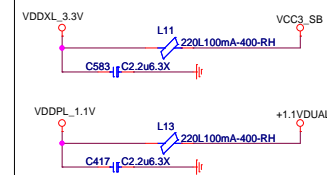
this pin is not used in external clock mode
(needed only for integrated clock)

MS-7900 use external clock GEN
So need to pull down

FCH DEBUG STRAPS (BOLTON-D4 HAS 15K INTERNAL PU FOR PCI_AD[30:23])

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL clock DEFAULT		normal REFCLK termination DEFAULT	Disable I2C ROM DEFAULT	Use ROMTYPE straps DEFAULT
PULL DOWN	Bypass Internal PLL clock		inverted REFCLK termination	Enable loading settings for UMI/PLL/misc from I2C ROM	Boot from PCI bus

+1.1VDUAL 1230mA

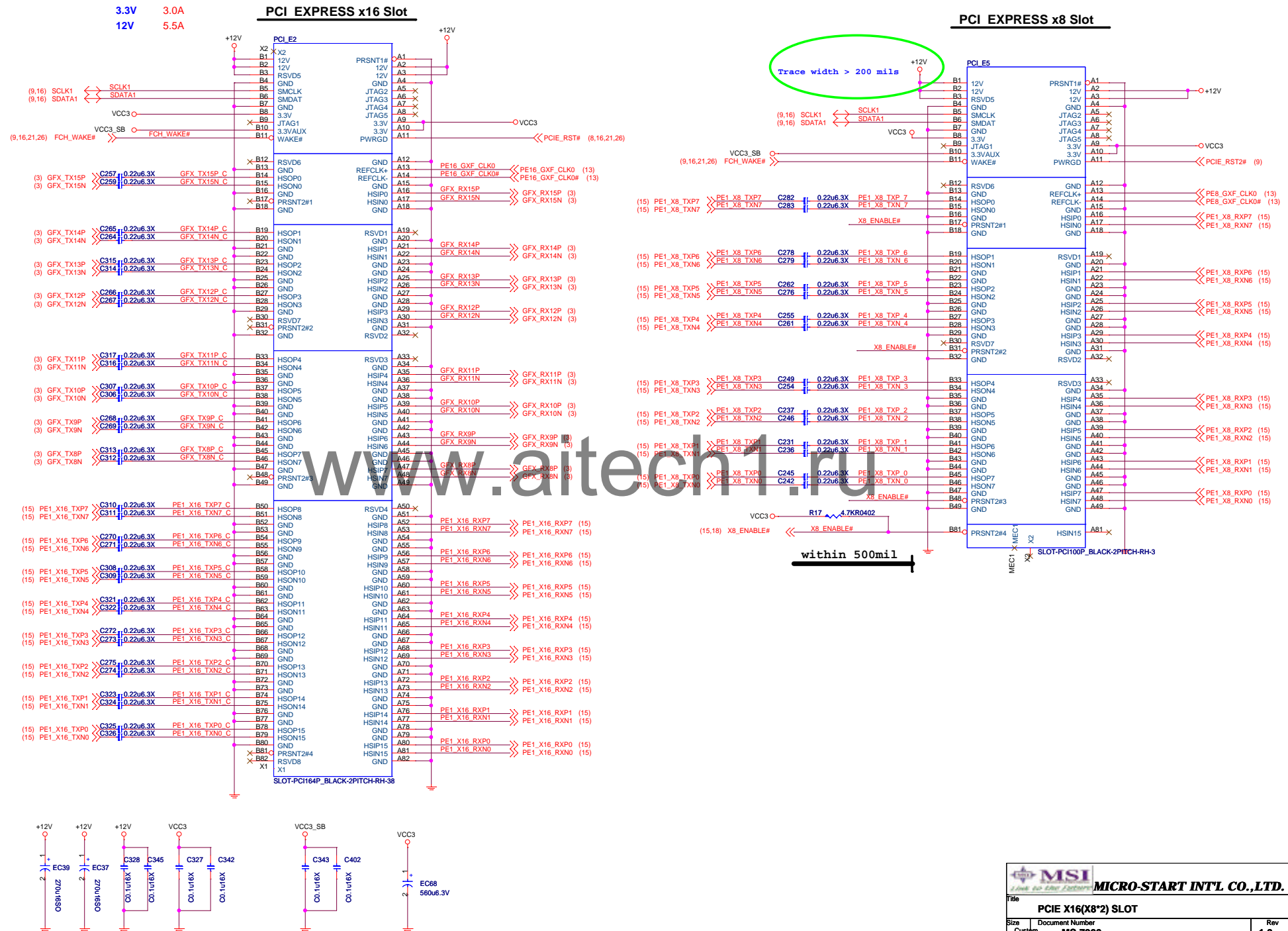


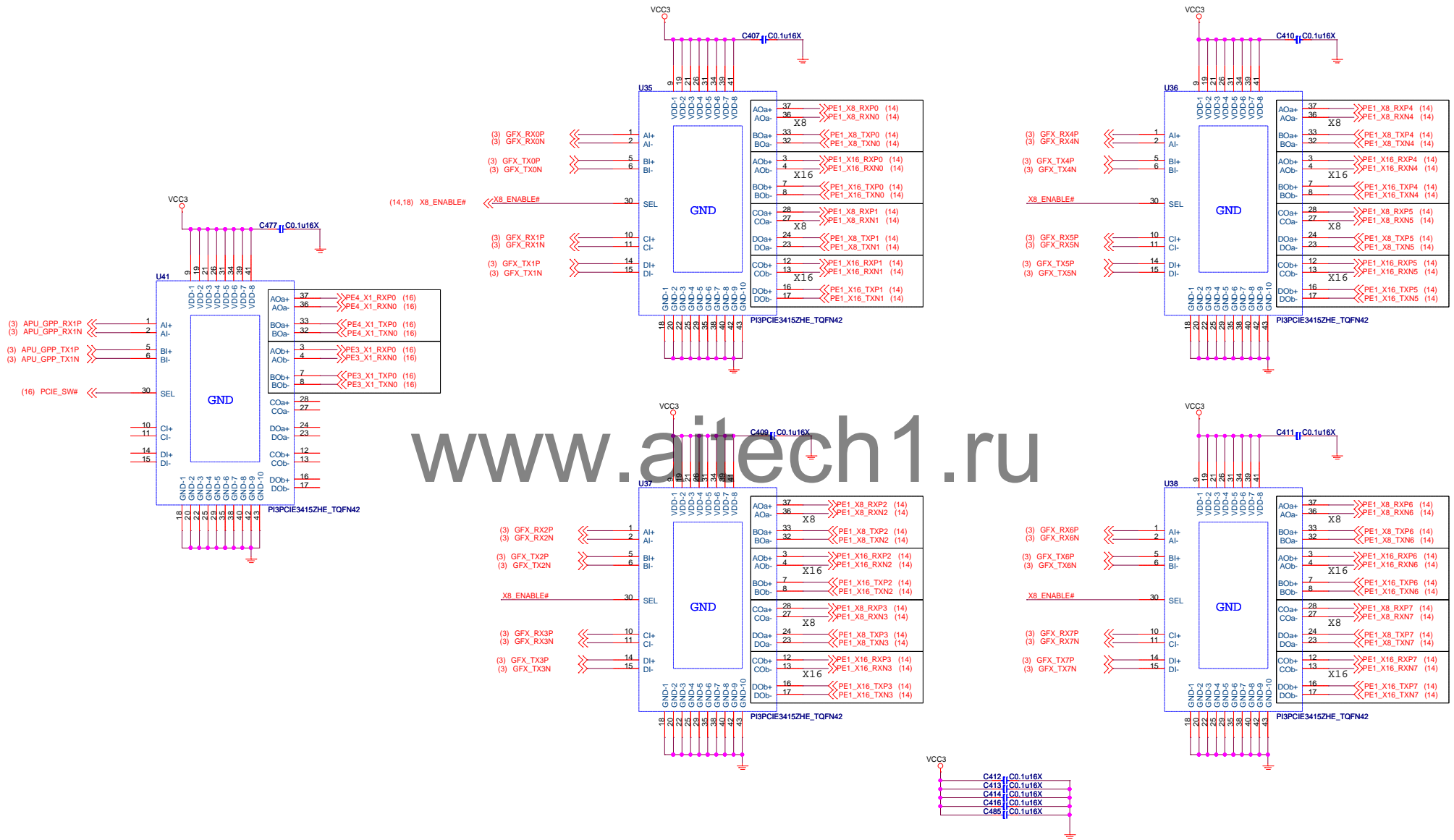
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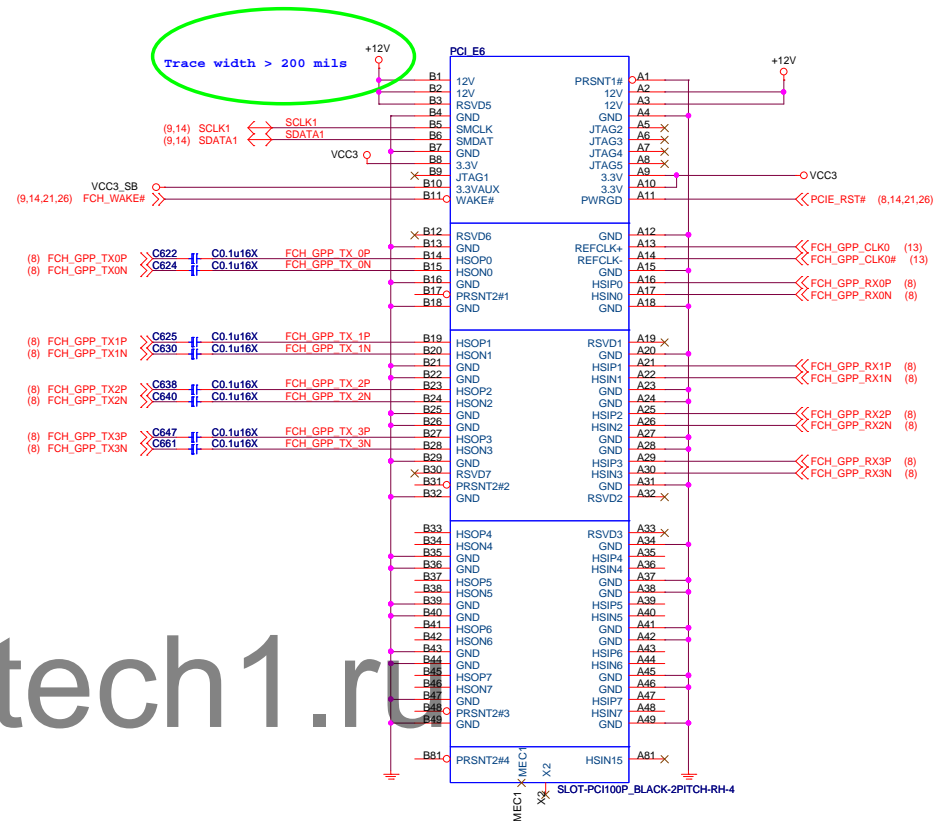
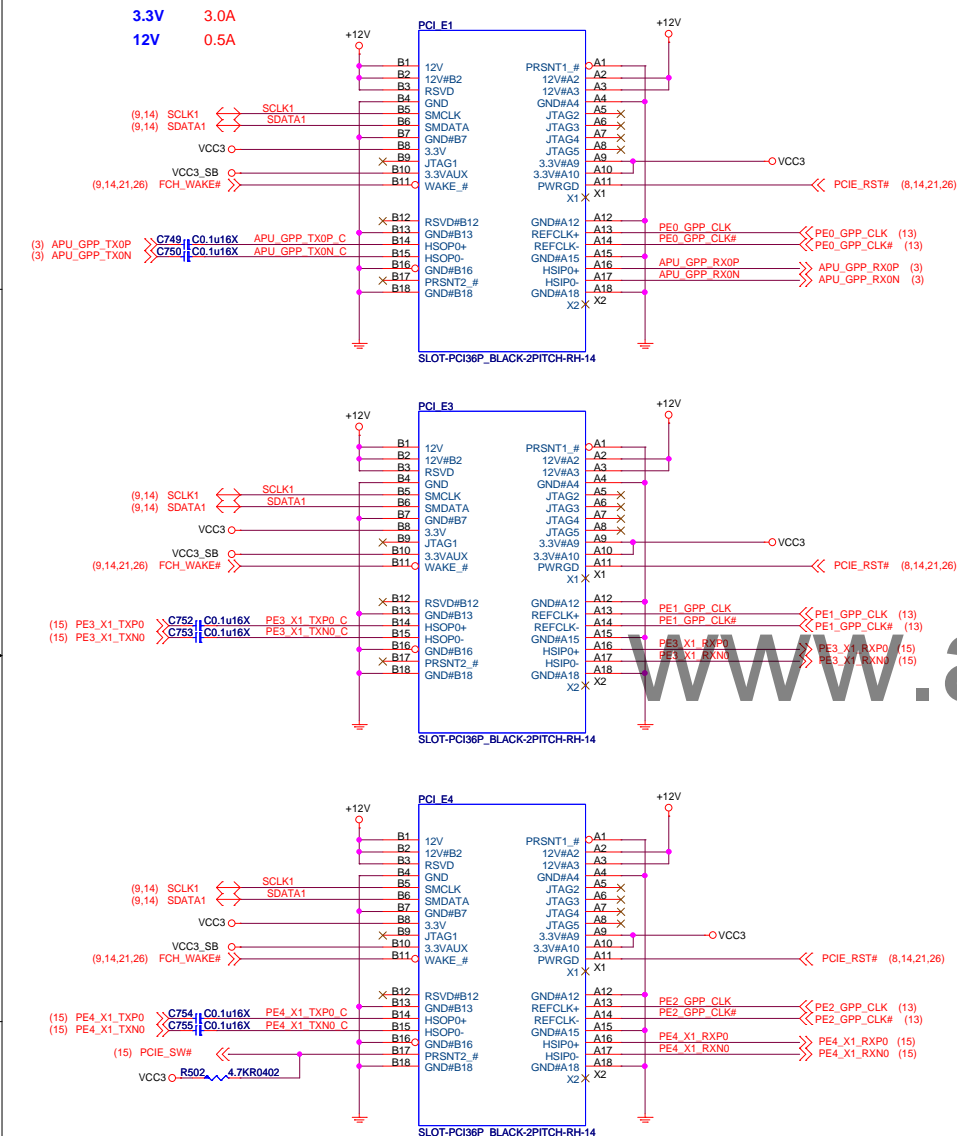
Select OC or non-OC mode Way 1







PCIEX1 12V 0.5A
3.3V weak 375mA

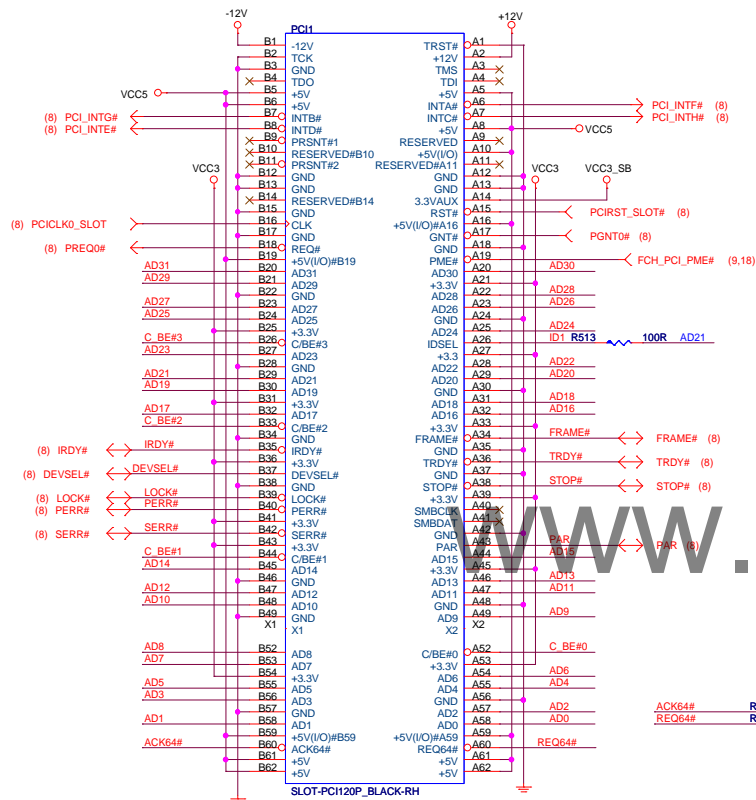


PCI Express X1 slot

+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

3.3V 7.6A
5V 5.0A
12V 0.5A

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

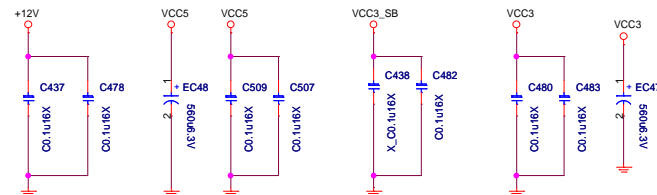


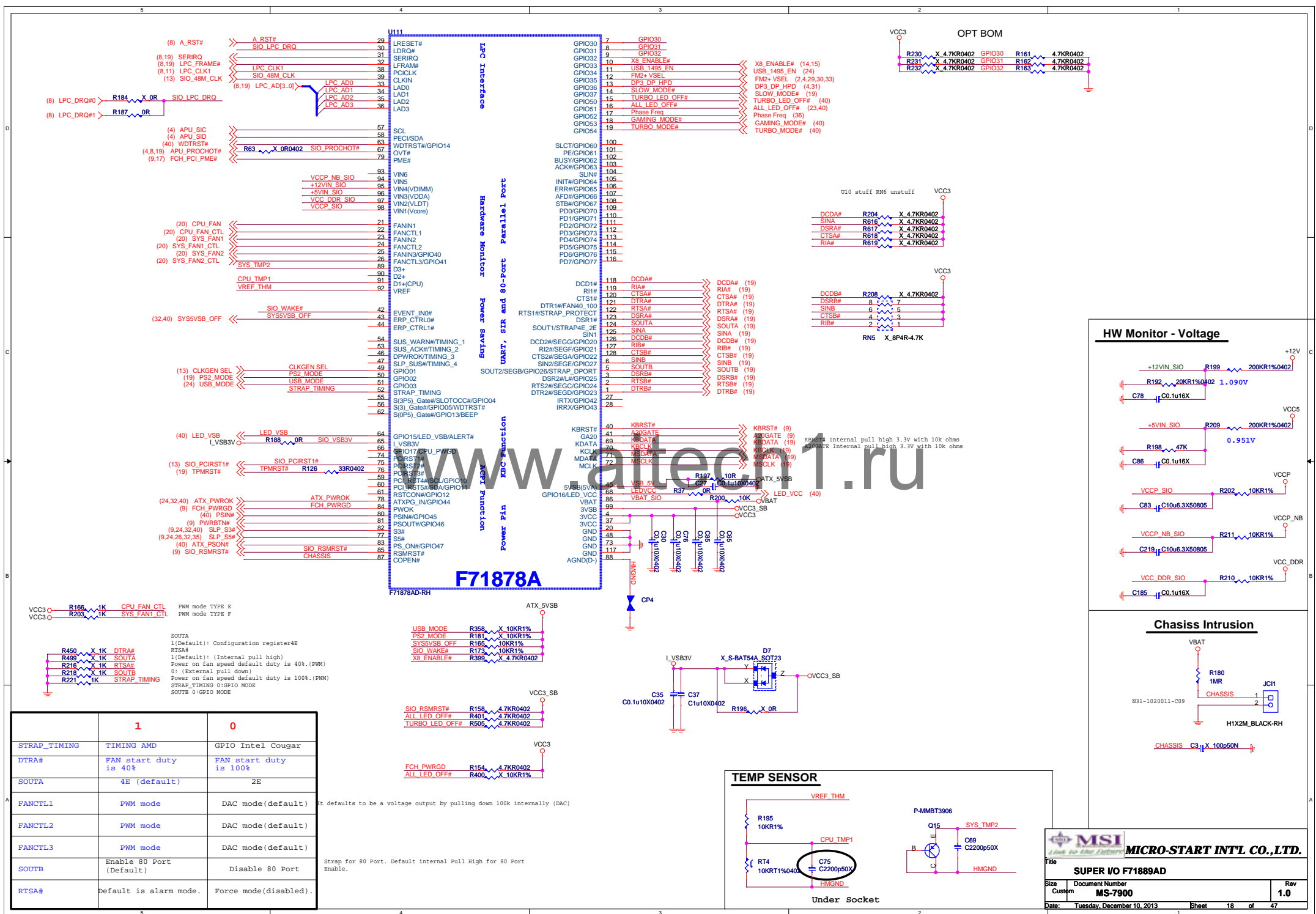
IDESEL = AD21

MASTER = PCI_REQ#0 PCI_GNT#0

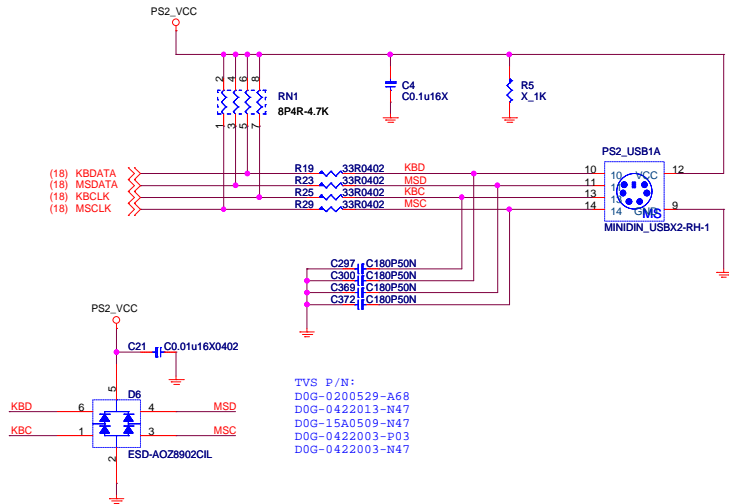
PCI Config.

DEVICE	MCP1 INT Pin	REQ# /GNT#	IDESEL	CLOCK
XXXXXX	PIRQ#E PIRQ#F PIRQ#G PIRQ#H		XXXX	CLK_33M_PCH_PCI (ICS113)
PCI Slot 1	PIRQ#F PIRQ#G PIRQ#H PIRQ#E	PREQ#0 PGNT#0	AD21	CLK_33M_PCH_PCI (ICS113)





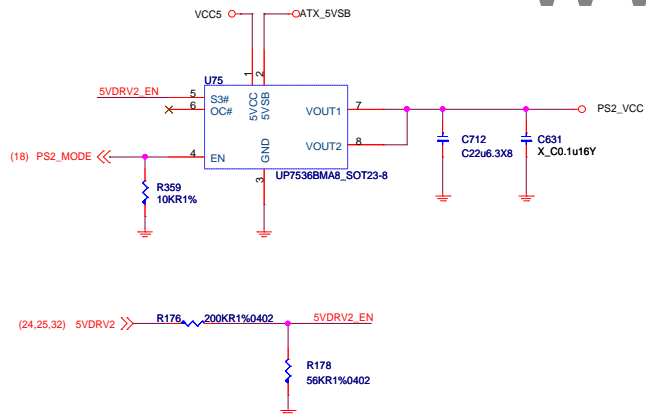
PS2 Connect



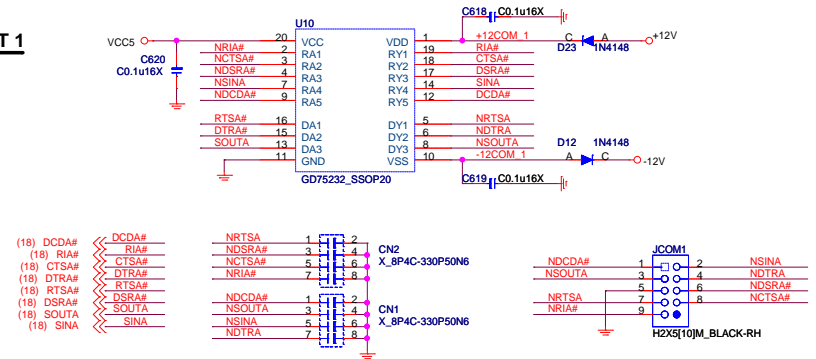
```

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

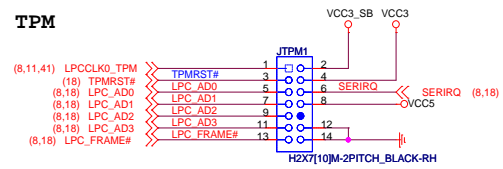
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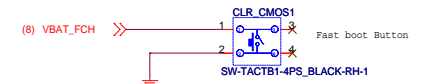
SERIAL PORT 1



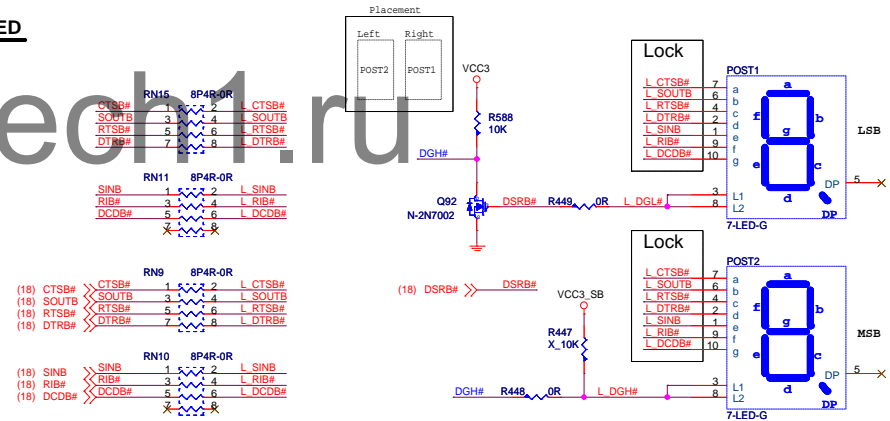
TPM



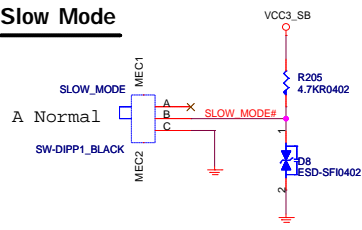
Clear CMOS button



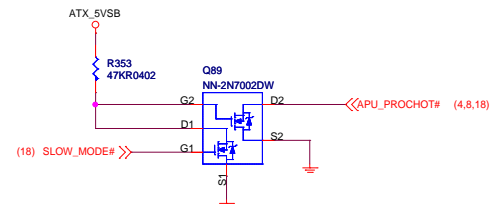
Debug LED



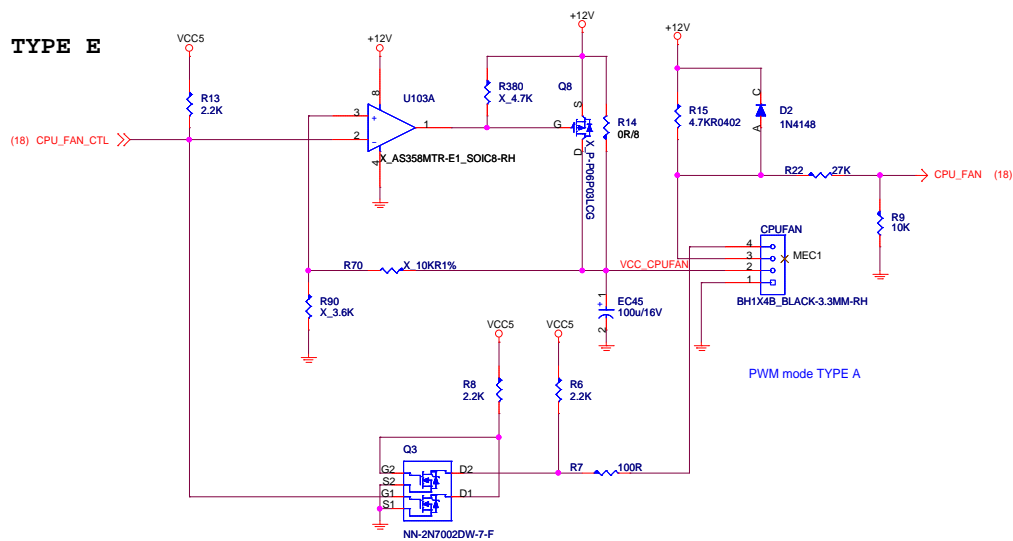
Slow Mode



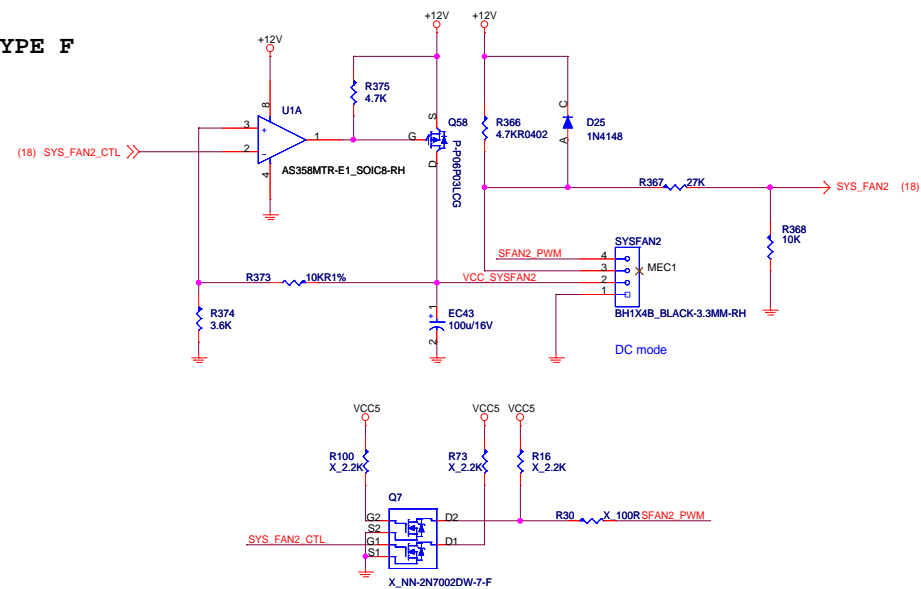
B Slow Mode



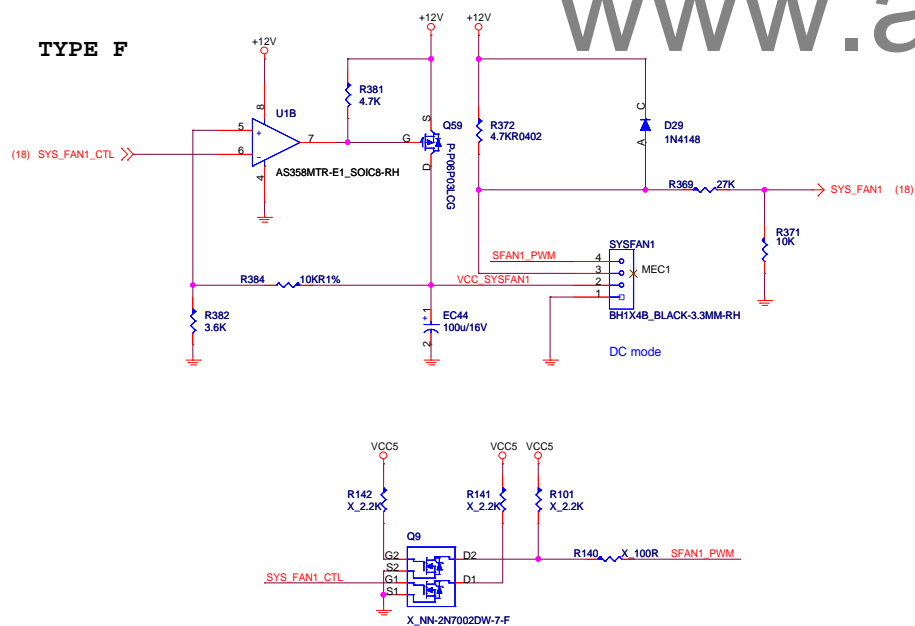
TYPE E



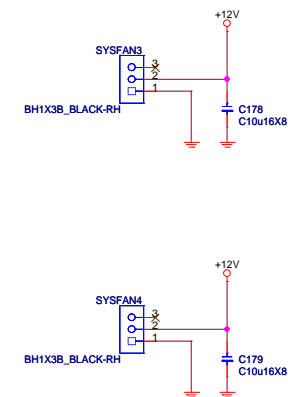
TYPE F



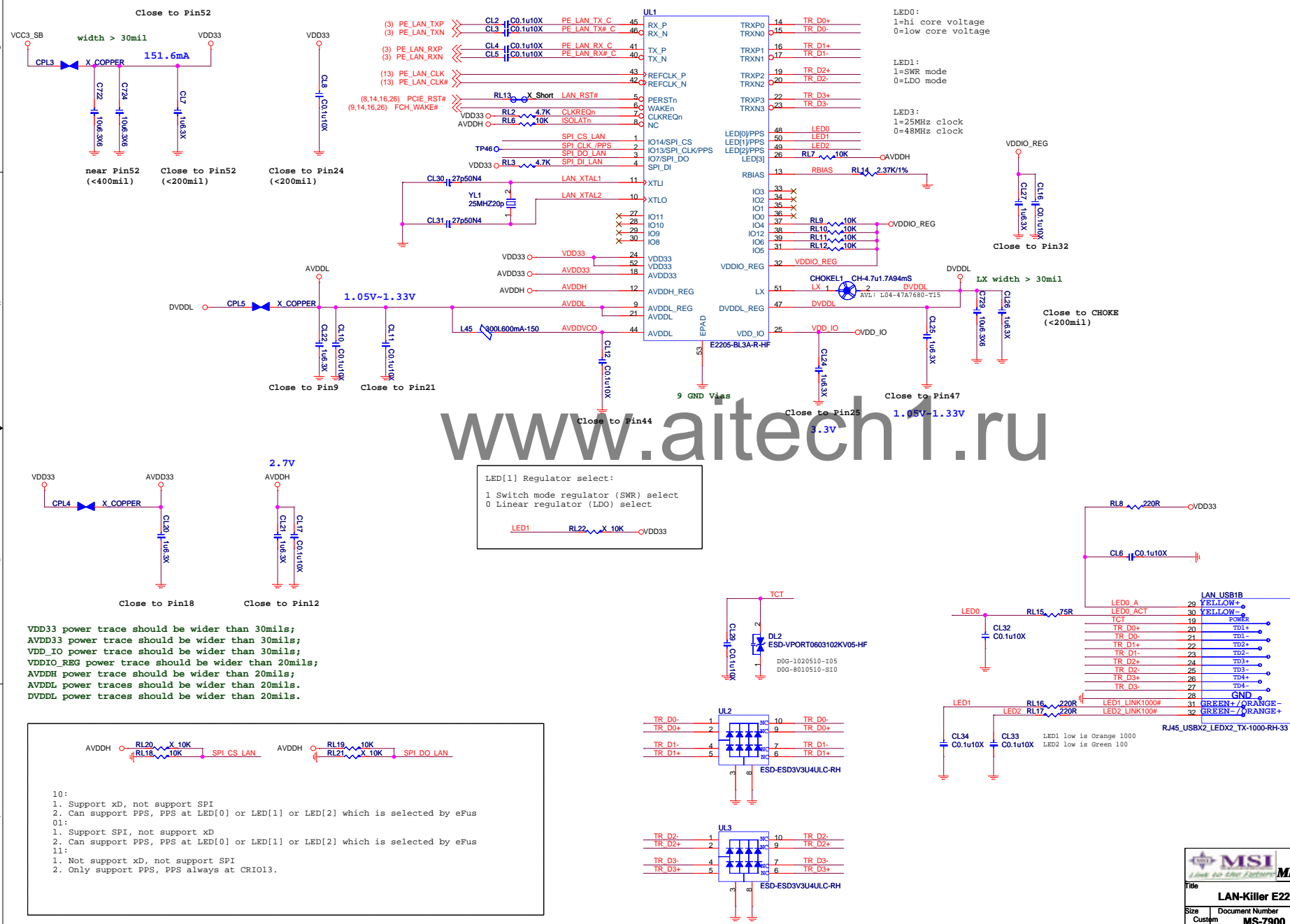
TYPE F



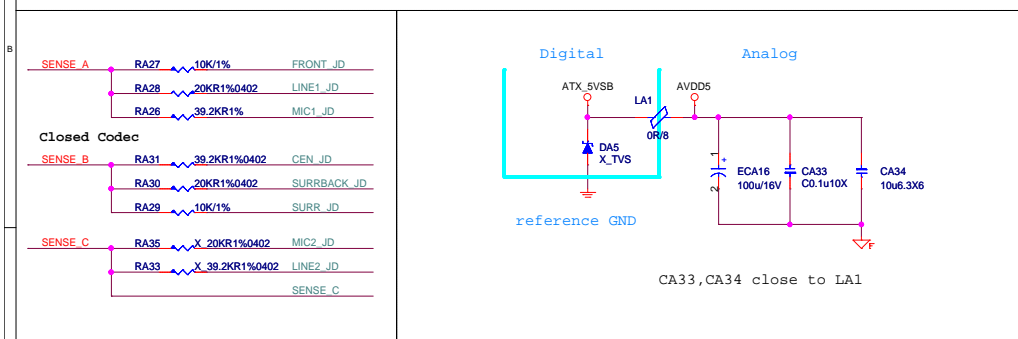
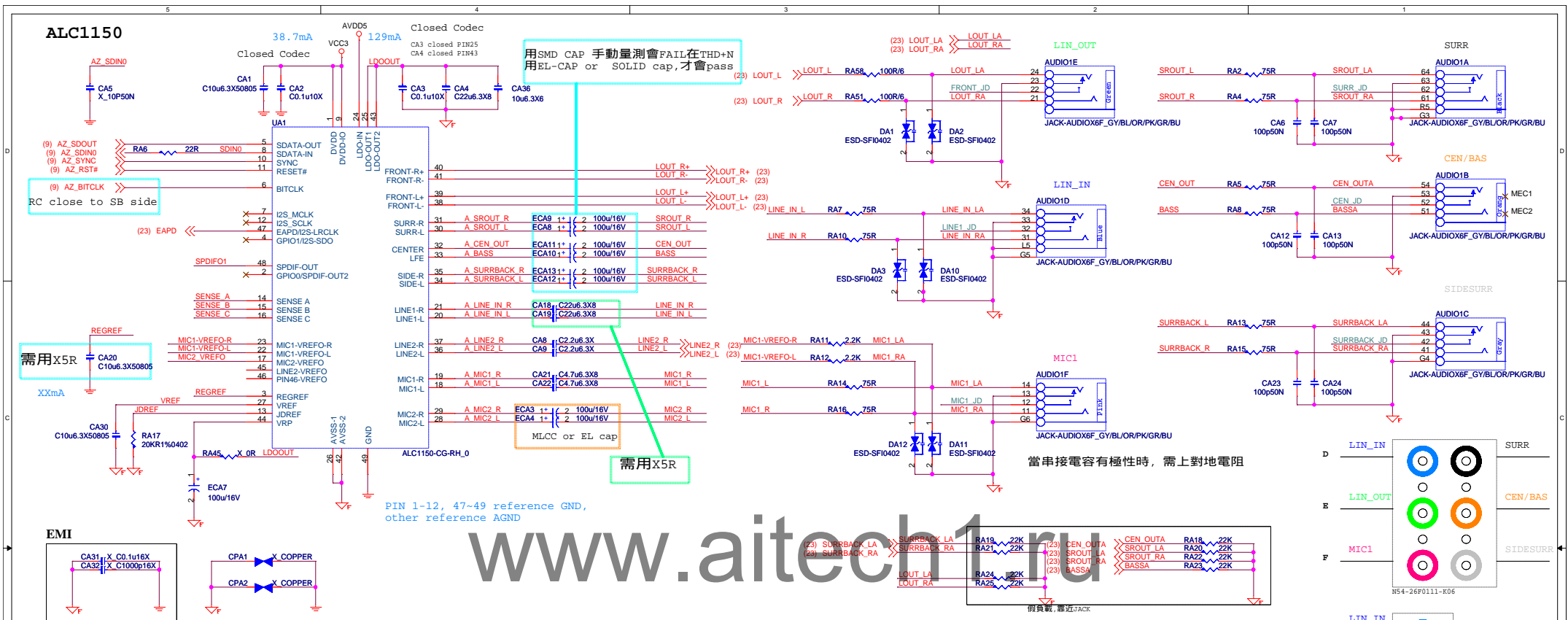
TYPE C



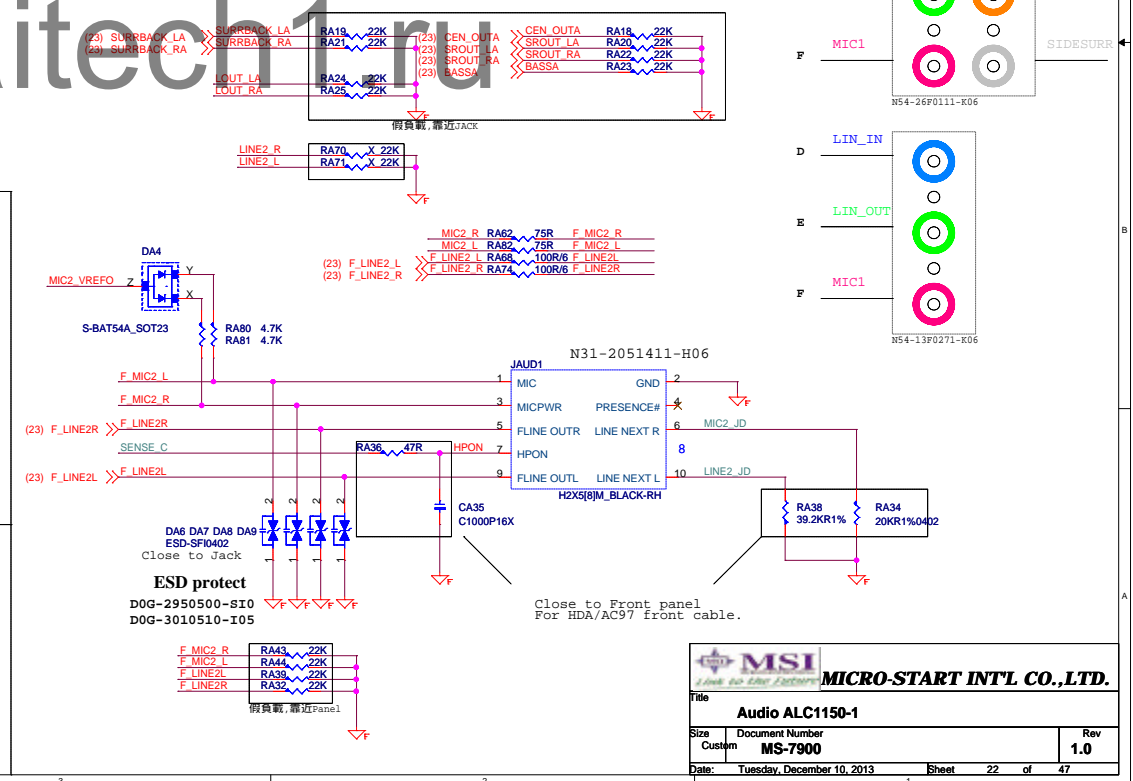
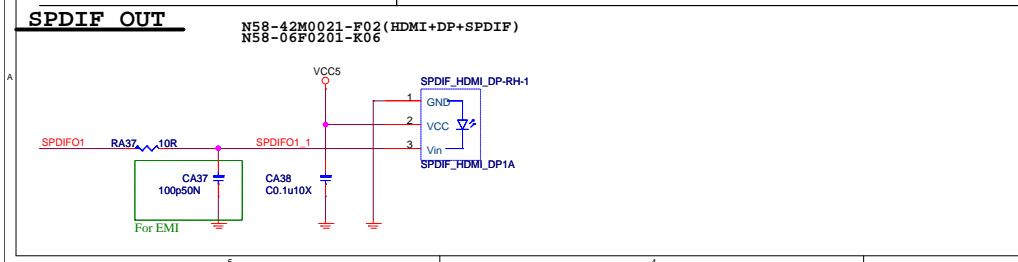
E2205-B Giga LAN

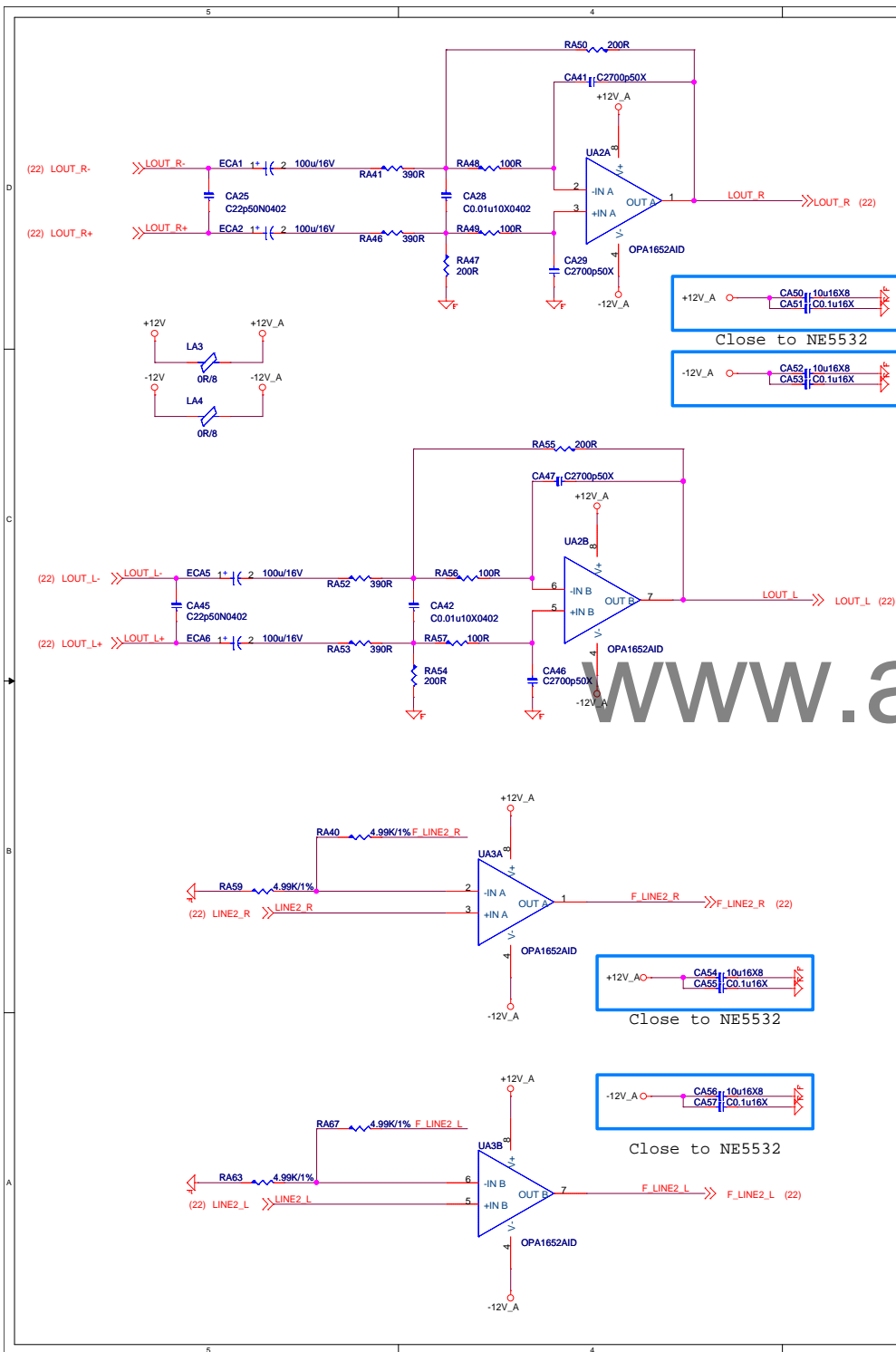


ALC1150

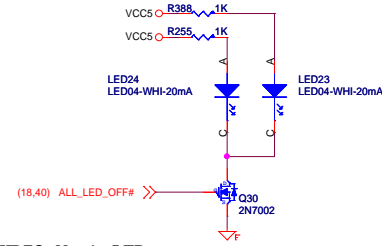


SPDIF OUT

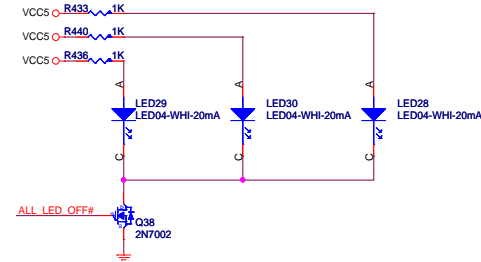




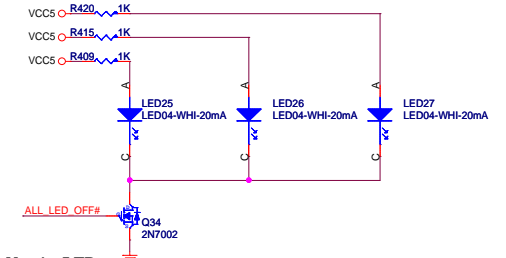
AUDIO Heatsink LED



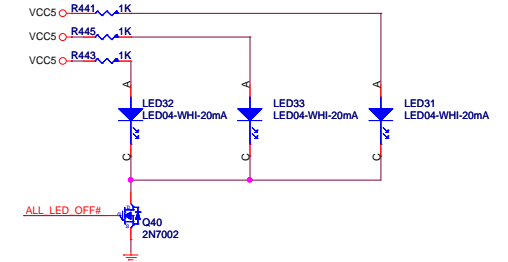
AUDIO Moat LED



AUDIO Moat LED

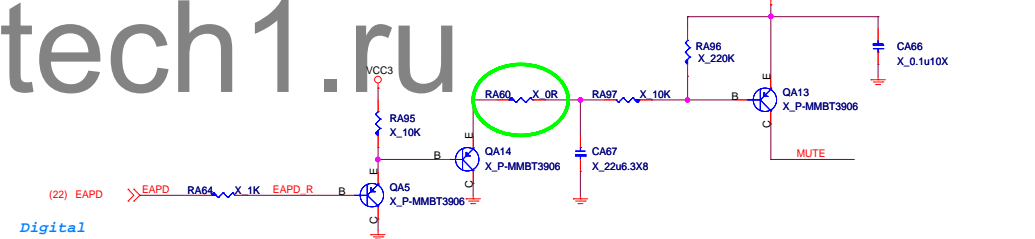


AUDIO Moat LED

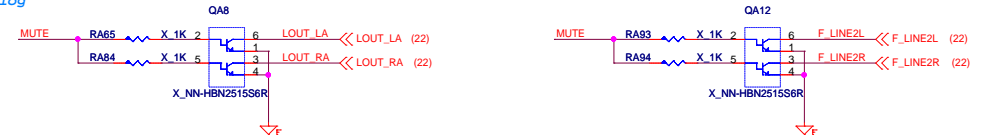


Rear Line OUT De-POP circuit

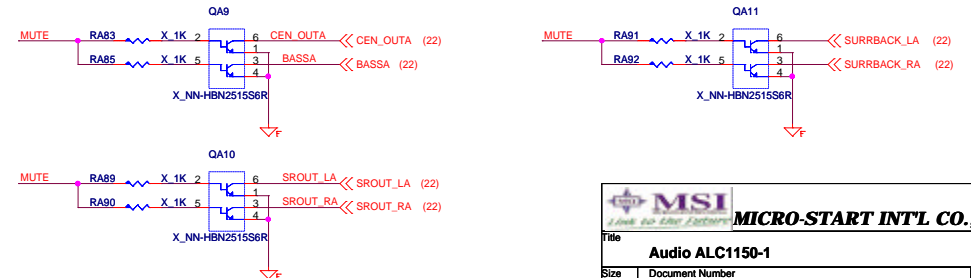
(reserve de-pop circuit for Rear Line out & Front Headphone out)



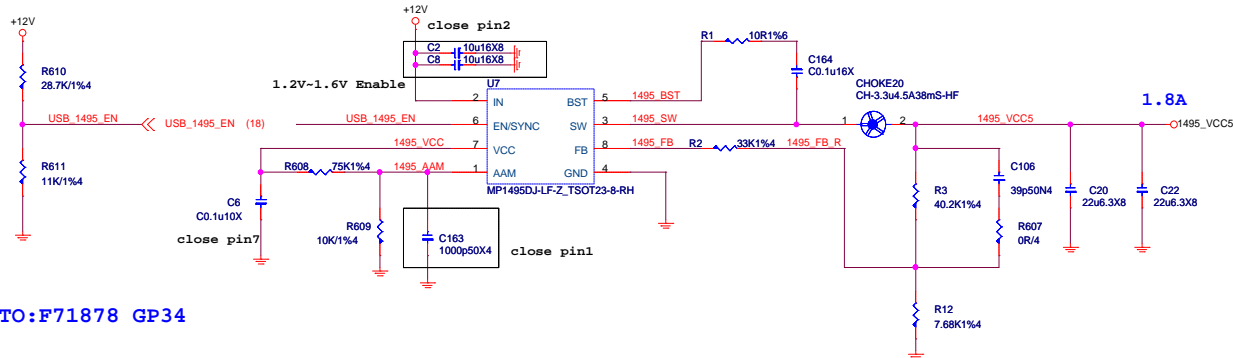
Analog



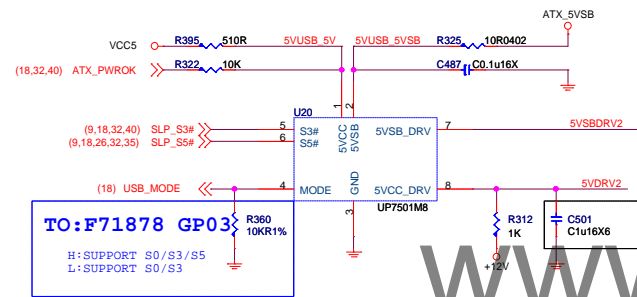
(add de-pop circuit by PM spec or customer request)



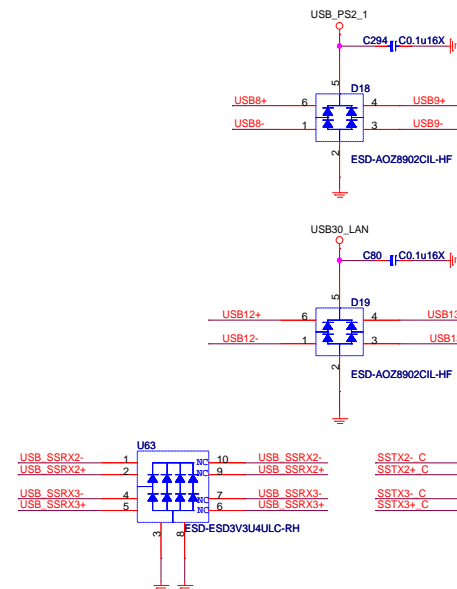
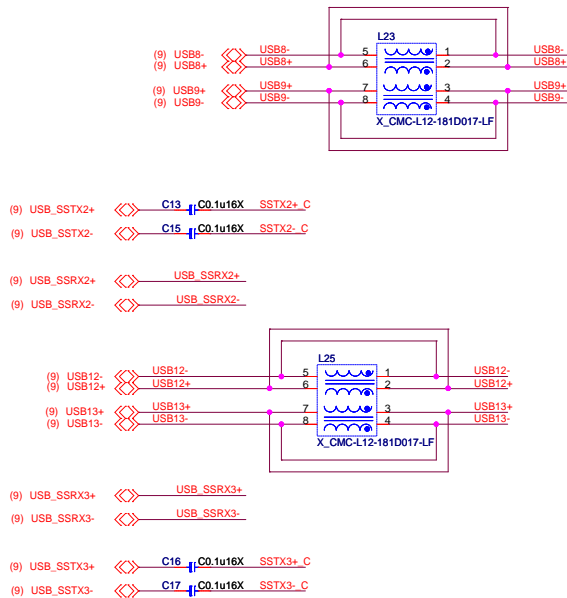
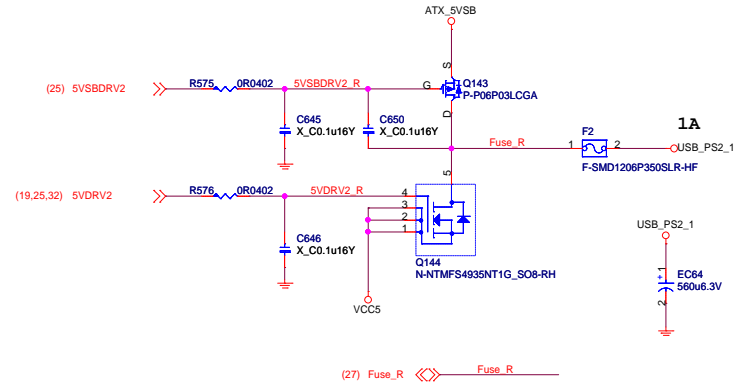
MP1495 USB Power



TO:F71878 GP34

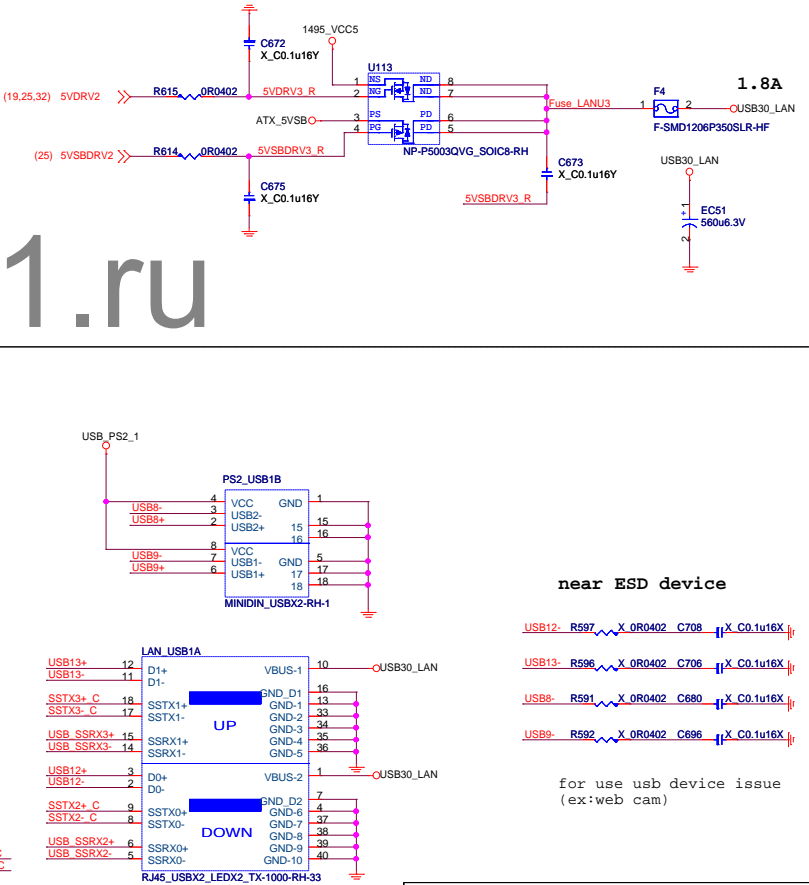


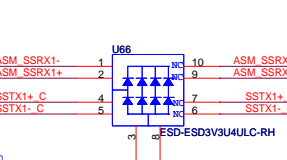
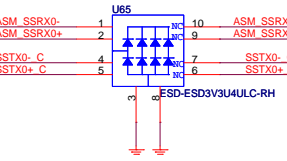
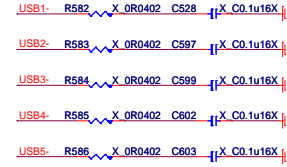
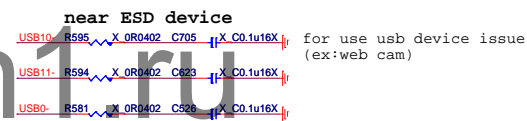
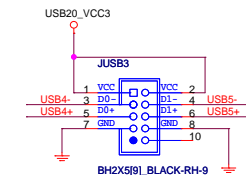
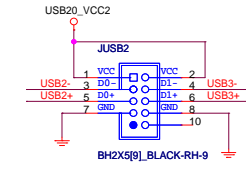
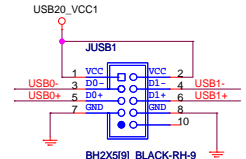
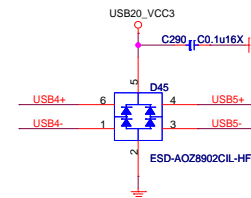
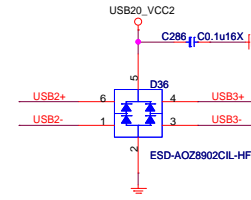
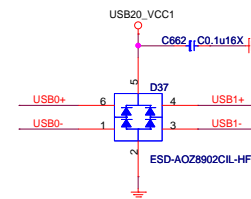
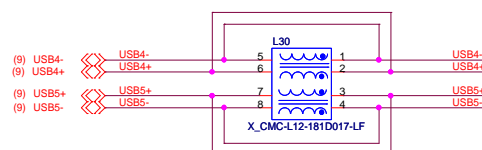
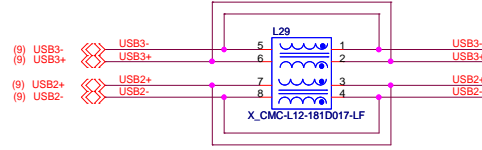
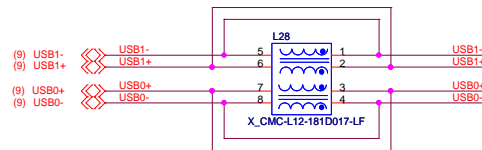
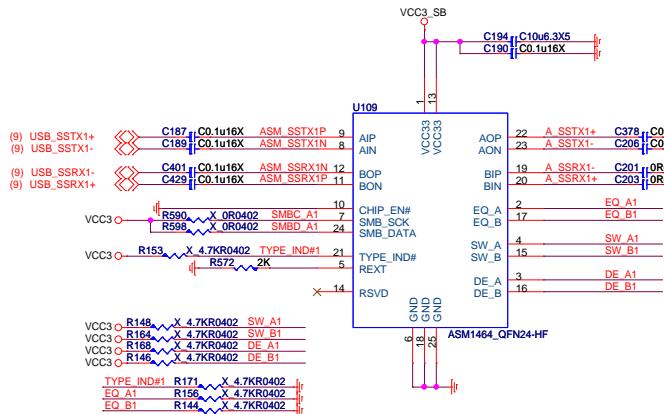
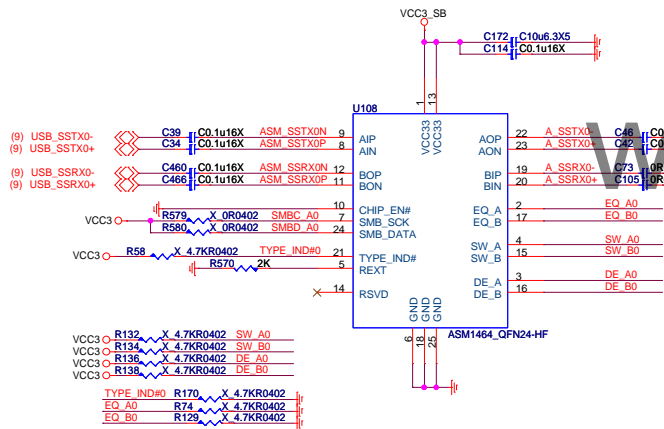
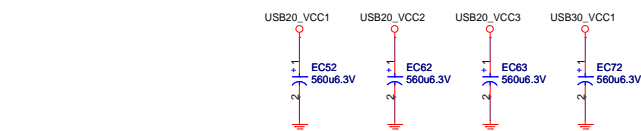
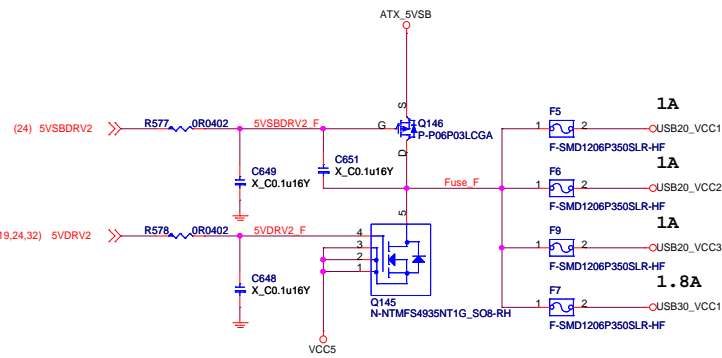
www.aitech1.ru



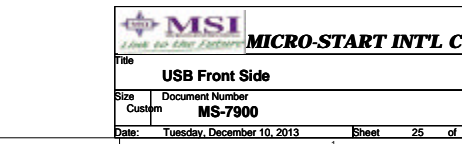
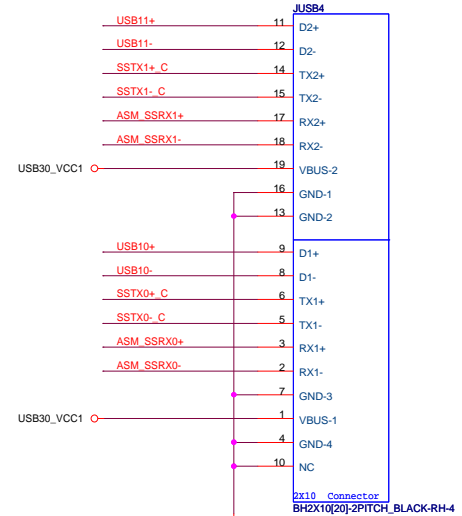
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

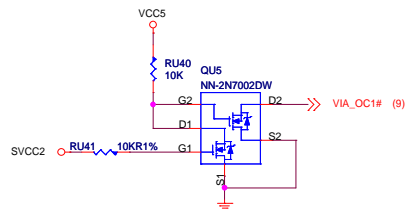
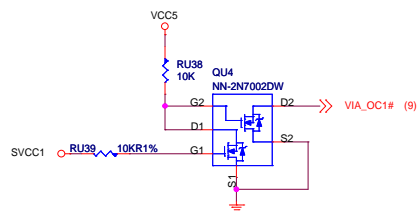
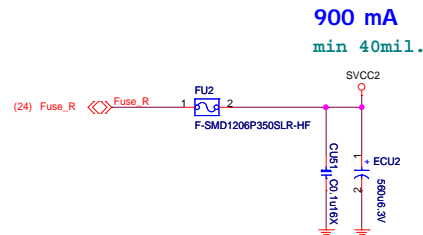
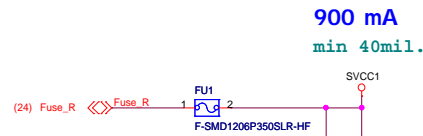
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL





near ESD device
for use usb device issue
(ex: web cam)

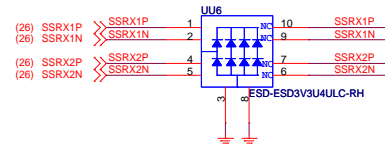
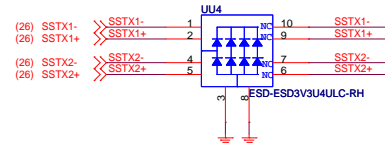




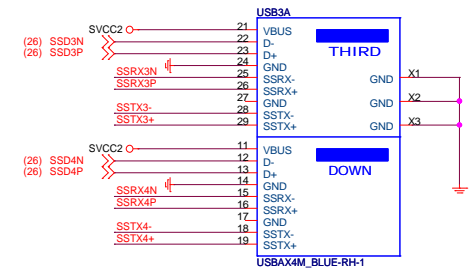
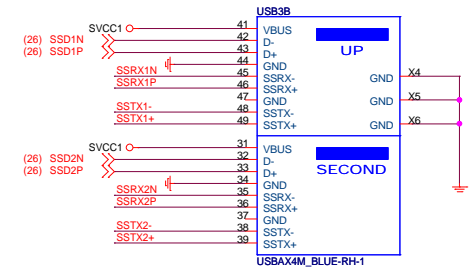
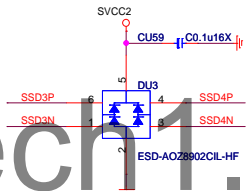
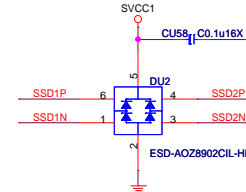
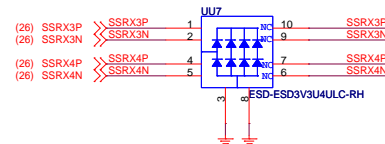
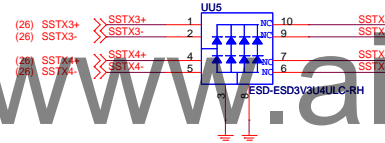
ESD Close to Connector

USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

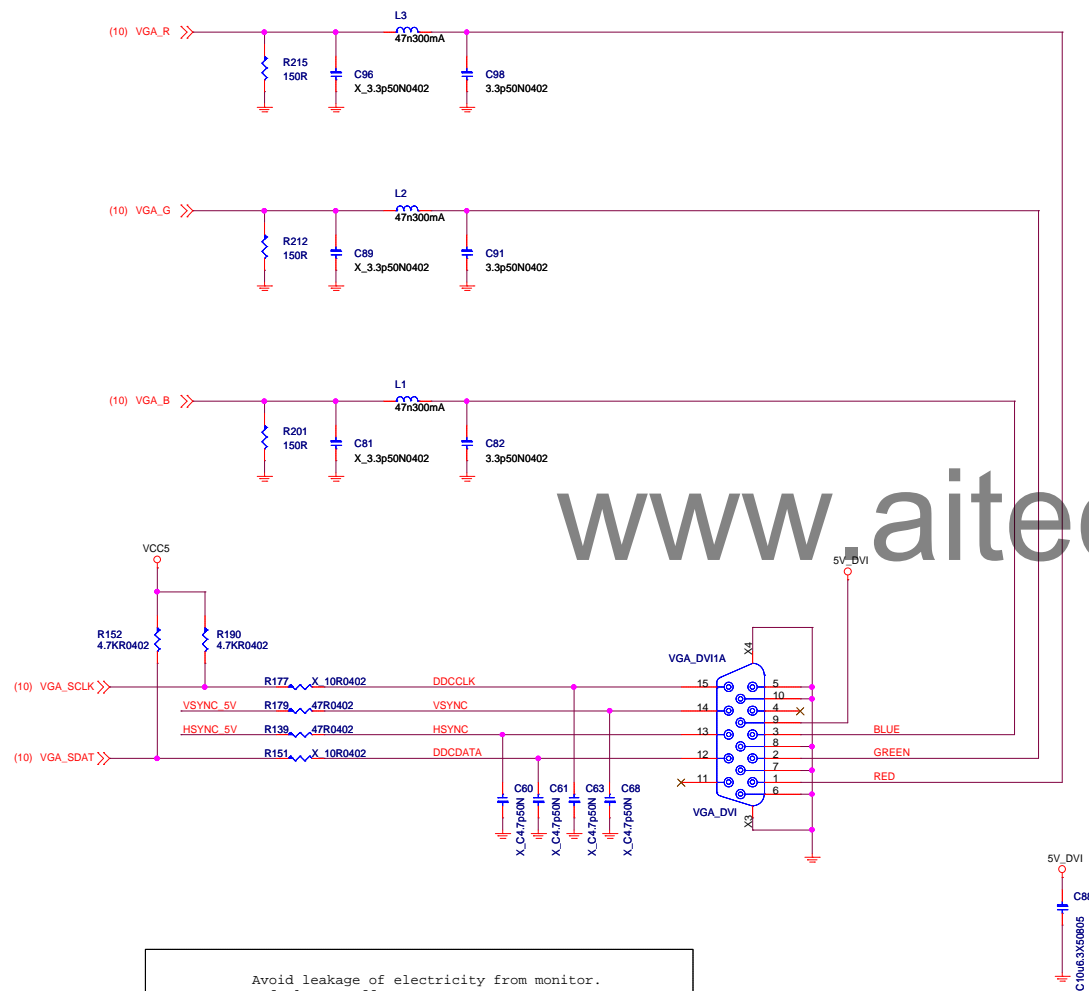
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL



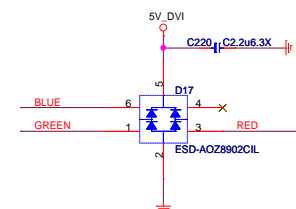
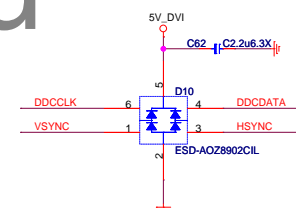
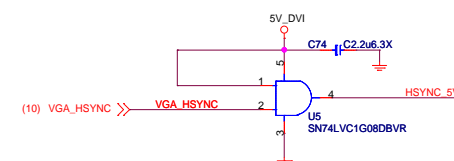
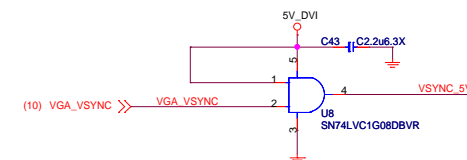
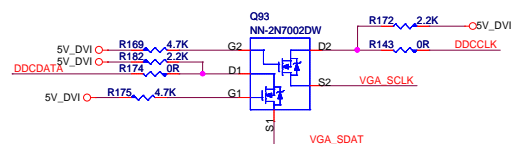
ESD Close to Connector



VGA CONNECTOR

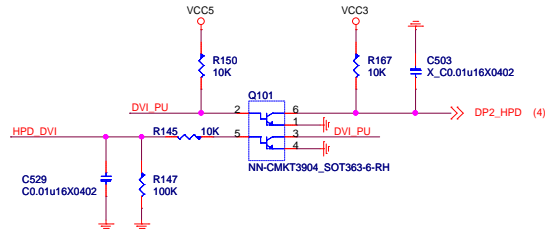


Avoid leakage of electricity from monitor.
Default unstuff.

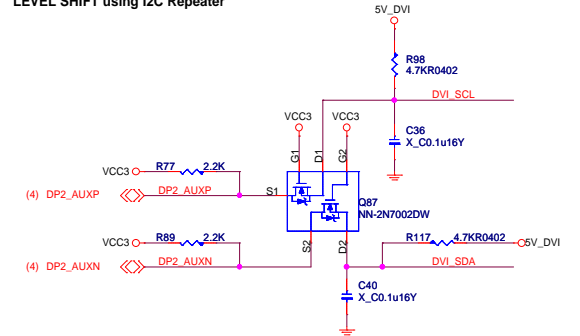


DVI CONNECTOR

(4) DP2_TX0N_APU	DP2_TX0N_APU	C121	C0.1u10X	DVI_TXD2-
(4) DP2_TX0P_APU	DP2_TX0P_APU	C124	C0.1u10X	DVI_TXD2+
(4) DP2_TX1N_APU	DP2_TX1N_APU	C115	C0.1u10X	DVI_TXD1-
(4) DP2_TX1P_APU	DP2_TX1P_APU	C118	C0.1u10X	DVI_TXD1+
(4) DP2_TX2N_APU	DP2_TX2N_APU	C111	C0.1u10X	DVI_TXD0-
(4) DP2_TX2P_APU	DP2_TX2P_APU	C103	C0.1u10X	DVI_TXD0+
(4) DP2_TX3N_APU	DP2_TX3N_APU	C134	C0.1u10X	DVI_TXC-
(4) DP2_TX3P_APU	DP2_TX3P_APU	C135	C0.1u10X	DVI_TXC+
(4) DP2_TX4N_APU	DP2_TX4N_APU	C139	C0.1u10X	DVI_TXD5-
(4) DP2_TX4P_APU	DP2_TX4P_APU	C136	C0.1u10X	DVI_TXD5+
(4) DP2_TX5N_APU	DP2_TX5N_APU	C127	C0.1u10X	DVI_TXD4-
(4) DP2_TX5P_APU	DP2_TX5P_APU	C131	C0.1u10X	DVI_TXD4+
(4) DP2_TX6N_APU	DP2_TX6N_APU	C141	C0.1u10X	DVI_TXD3-
(4) DP2_TX6P_APU	DP2_TX6P_APU	C138	C0.1u10X	DVI_TXD3+

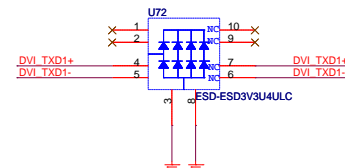
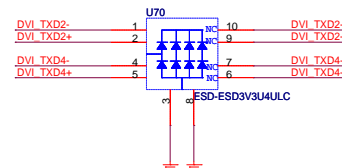
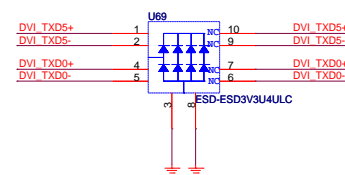
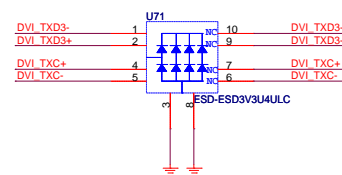
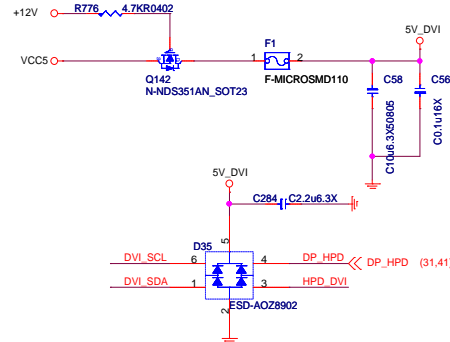
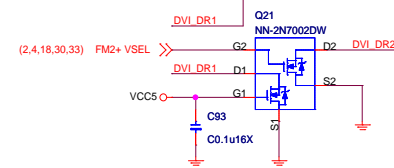
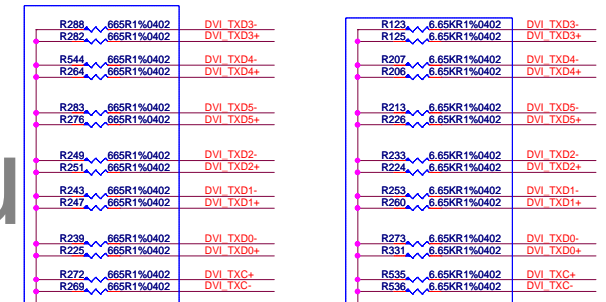


LEVEL SHIFT using I2C Repeater



2012/03/20 Change DVI(TMD5) terminations from 715ohm to 604ohm

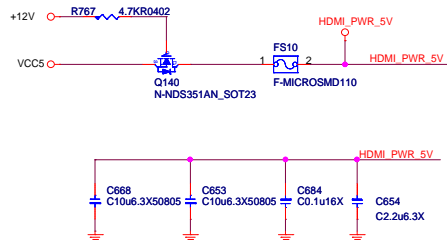
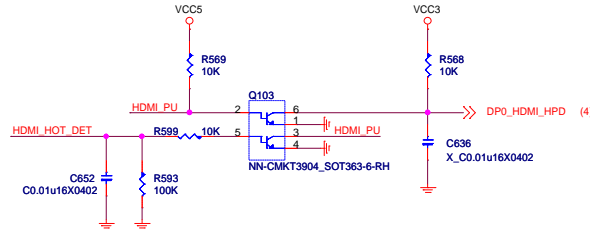
2013/03/01 Co-lay FM2+ need change DVI(TMD5) terminations from 604ohm to 665ohm



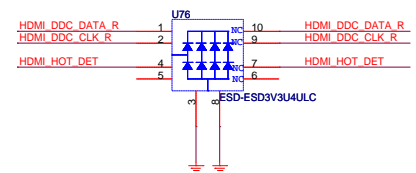
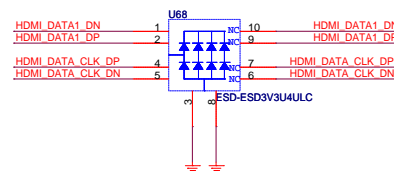
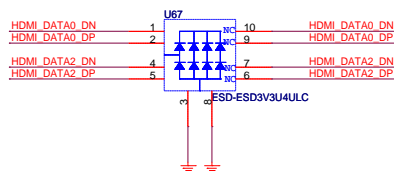
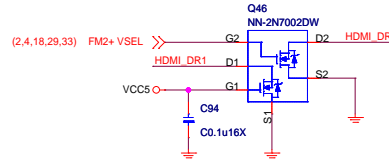
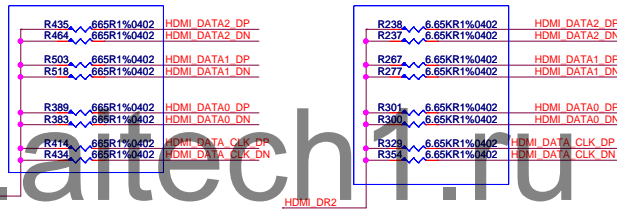
HDMI CONNECTOR

(4) DP0_TX0P_APU	>>>	DP0_TX0P_APU	C513	C0.1u16X	HDMI_DATA2_DP
(4) DP0_TX0N_APU	>>>	DP0_TX0N_APU	C518	C0.1u16X	HDMI_DATA2_DN
(4) DP0_TX1P_APU	>>>	DP0_TX1P_APU	C520	C0.1u16X	HDMI_DATA1_DP
(4) DP0_TX1N_APU	>>>	DP0_TX1N_APU	C522	C0.1u16X	HDMI_DATA1_DN
(4) DP0_TX2P_APU	>>>	DP0_TX2P_APU	C523	C0.1u16X	HDMI_DATA0_DP
(4) DP0_TX2N_APU	>>>	DP0_TX2N_APU	C580	C0.1u16X	HDMI_DATA0_DN
(4) DP0_TX3P_APU	>>>	DP0_TX3P_APU	C621	C0.1u16X	HDMI_DATA_CLK_DP
(4) DP0_TX3N_APU	>>>	DP0_TX3N_APU	C626	C0.1u16X	HDMI_DATA_CLK_DN

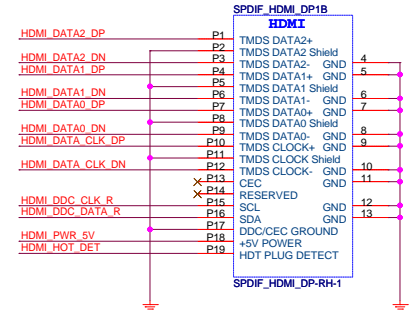
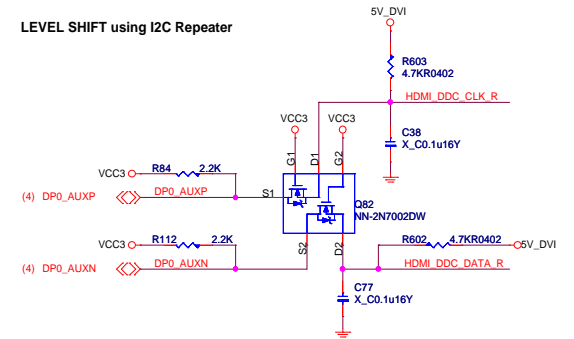
HDMI_DATA0_DP	R299	X_OR0402
HDMI_DATA0_DN		
HDMI_DATA1_DP	R313	X_OR0402
HDMI_DATA1_DN		
HDMI_DATA2_DP	R370	X_OR0402
HDMI_DATA2_DN		
HDMI_DATA_CLK_DP	R378	X_OR0402
HDMI_DATA_CLK_DN		



2012/03/20 Change DVI(TMDS) terminations from 715ohm to 604ohm
2013/03/01 Co-Lay FM2+ need change DVI(TMDS) terminations from 604ohm to 665ohm



LEVEL SHIFT using I2C Repeater

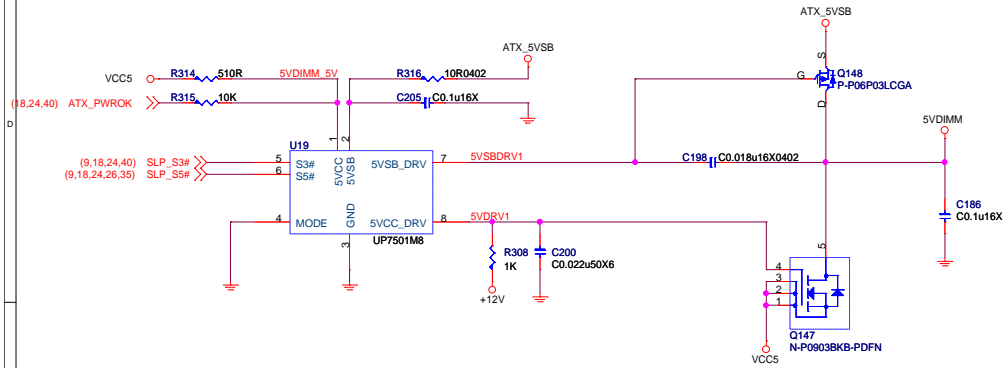


[illegible]

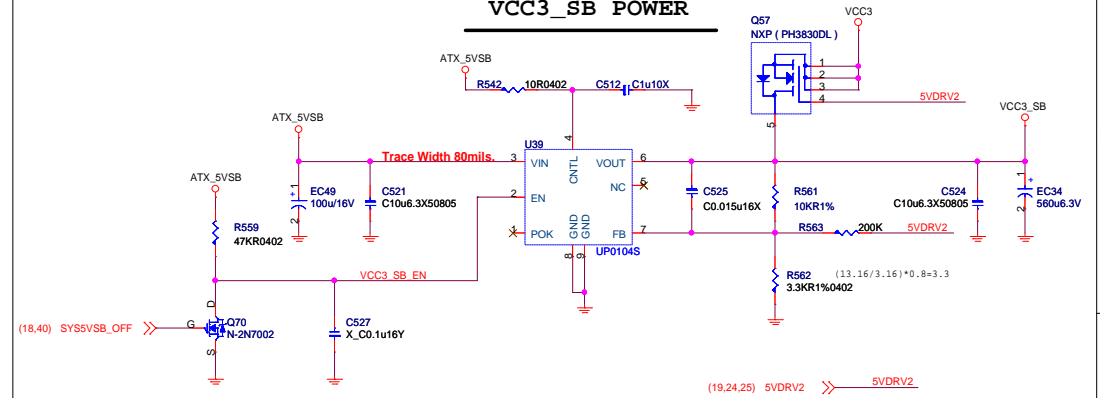
1=VGA

DP_VGA# (SEL pin)	L	Dx to Dx A	DP
	H	Dx to Dx B	VGA (Default)

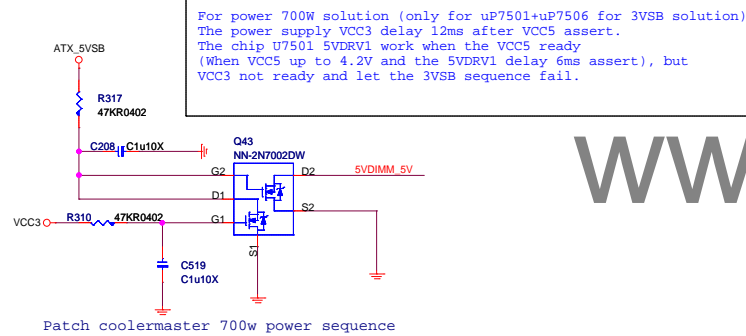
5VDIMM FOR DDR



VCC3_SB POWER



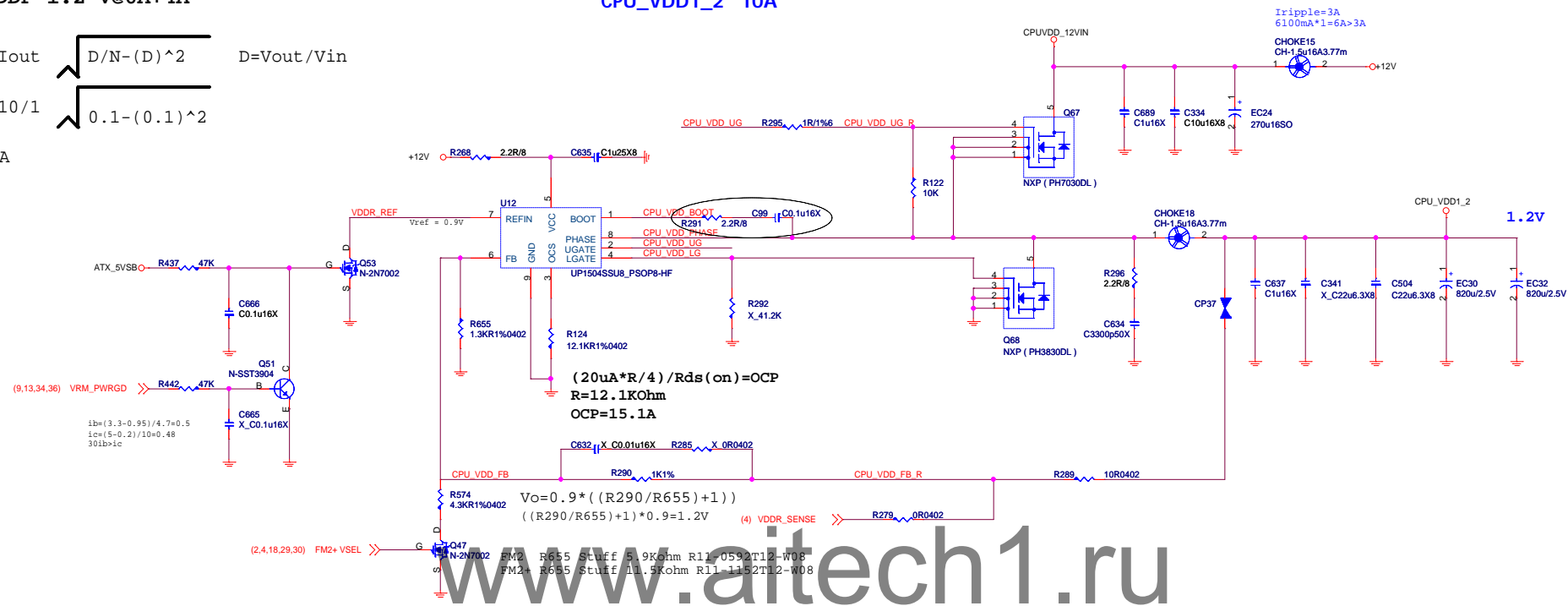
For special PSU sequence



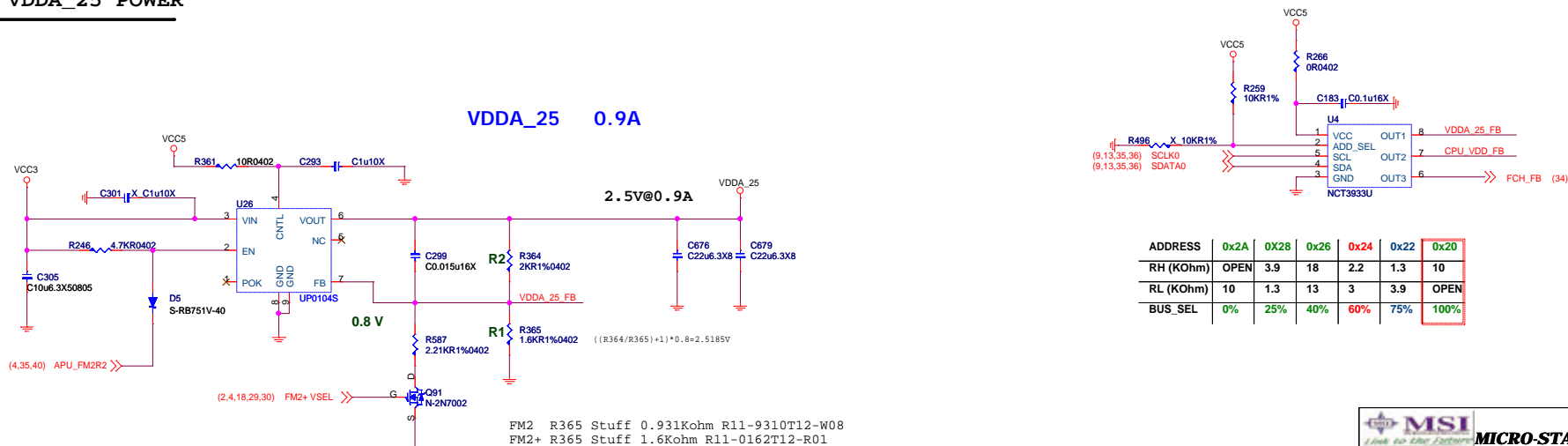
DIS CHARGE

CPU_VDD1_2 10A

$$\begin{aligned} I_{rms} &= I_{out} \sqrt{D/N - (D)^2} & D &= V_{out}/V_{in} \\ &= 10/1 \sqrt{0.1 - (0.1)^2} \\ &= 3A \end{aligned}$$

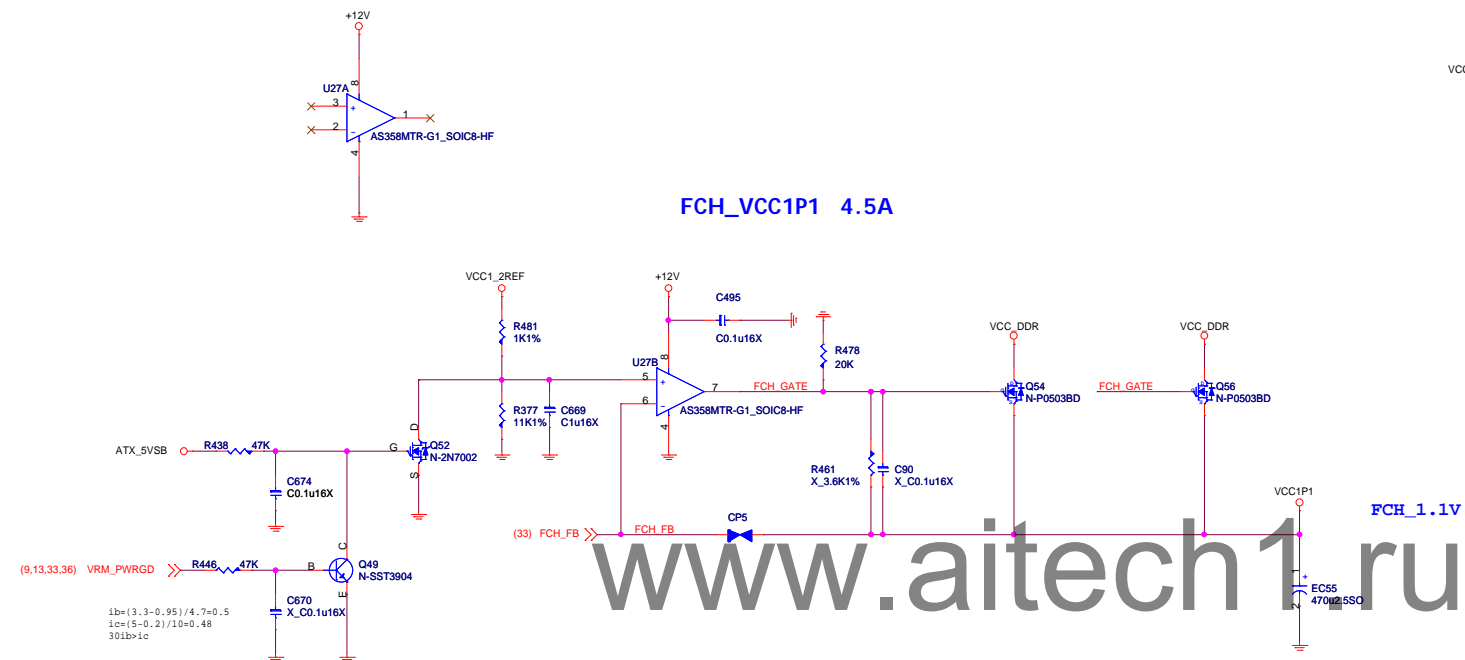


VDDA_25 0.9A

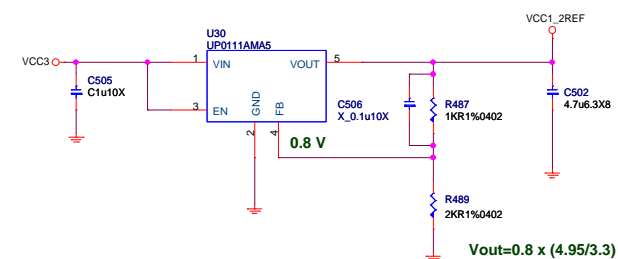


ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	18	2.2	1.3	10
RL (KOhm)	10	1.3	13	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

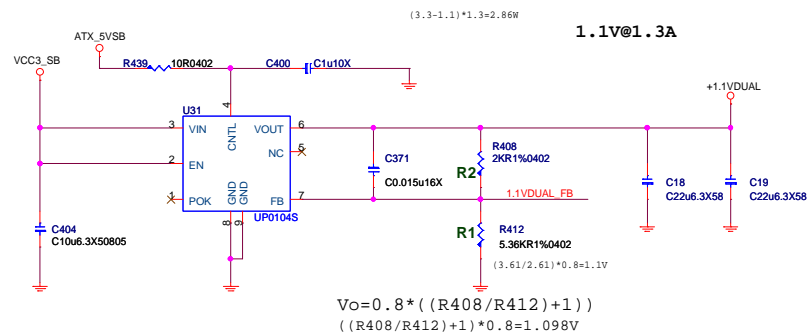
FCH VCC1P1 POWER
FCH_VCC1P1 V@4.5A



VCC1_2REF

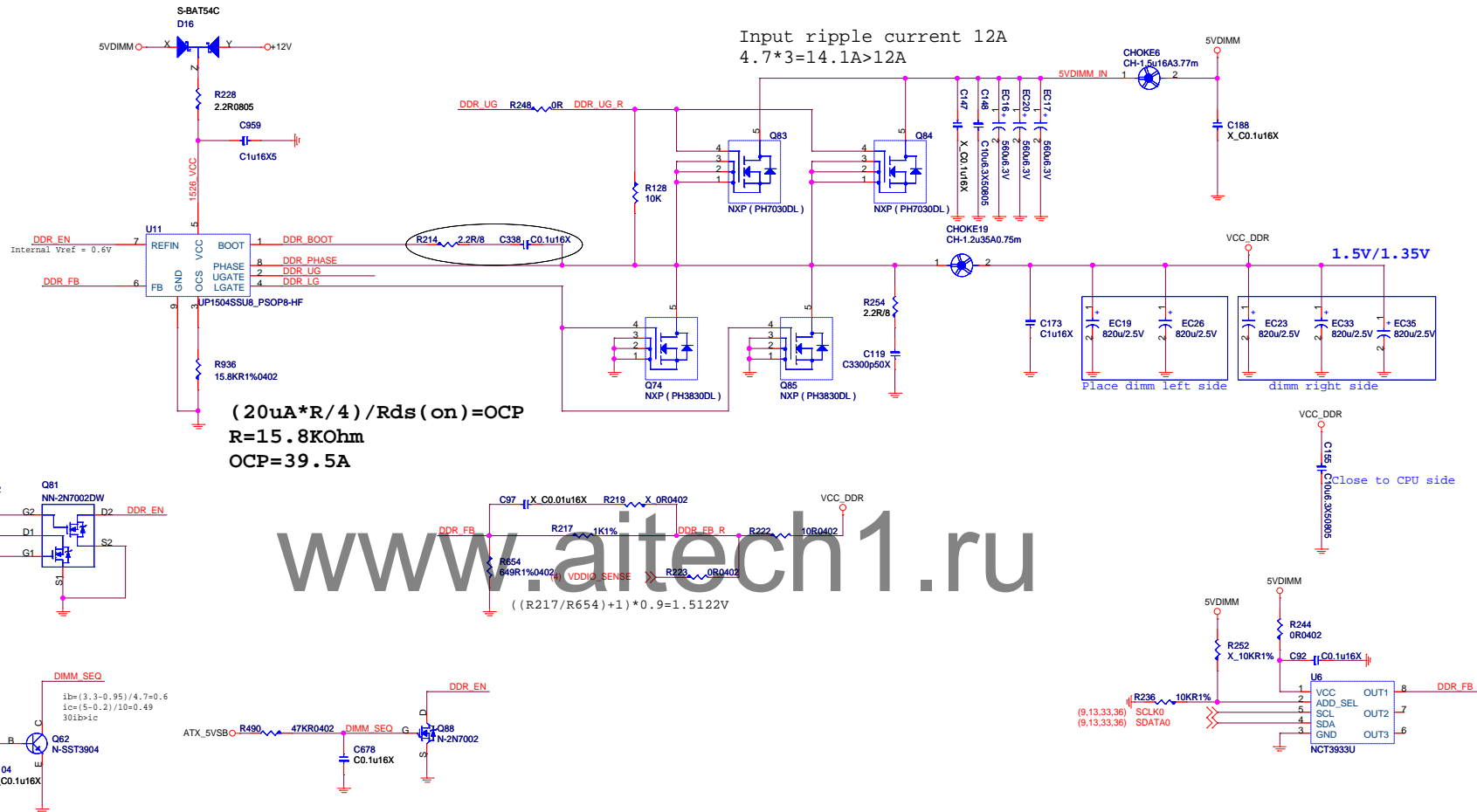


FCH +1.1VDUAL POWER



$$I_{rms} = I_{out} \sqrt{D/N - (D)^2} = 22/1 \sqrt{0.3 - (0.3)^2} = 10.08A$$

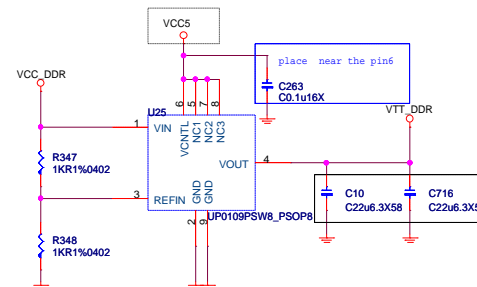
DDR III 1.5V POWER
VCC_DDR 15A+5A+4.4



ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	18	2.2	1.3	10
RL (KOhm)	10	1.3	13	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

VTT_DDR POWER 0.75V@4A

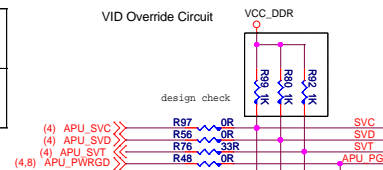
VTT_DDR 0.5A*4=2A



MODE	DDR_WF		
第一階(Default)	HIGH		WF=200KHz
第二階	LOW		WF=400KHz

Note:

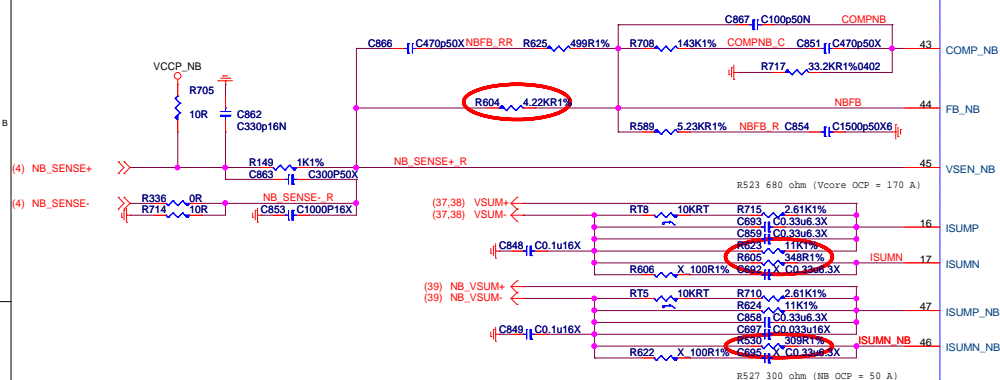
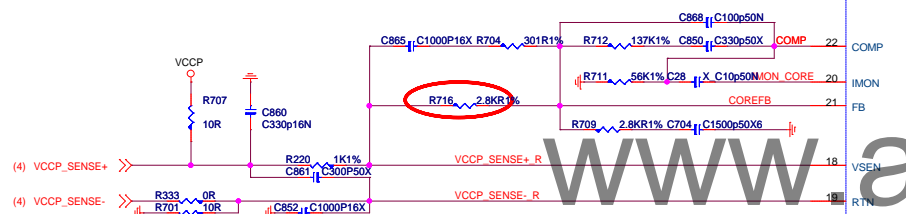
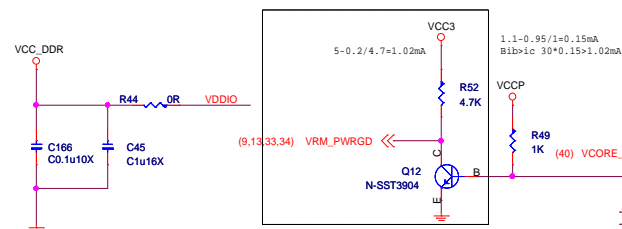
		BOOT VOLTAGE
SVC	SVD	Pre PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



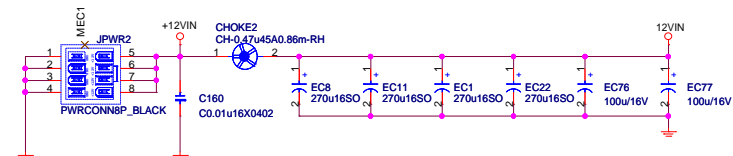
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APU_PG:
from FCH to APU & UP1640
PU 330R to VCC_DDR

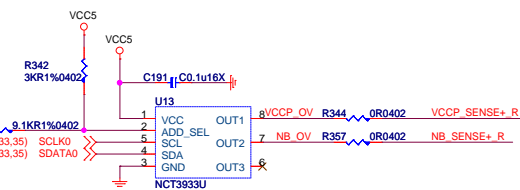
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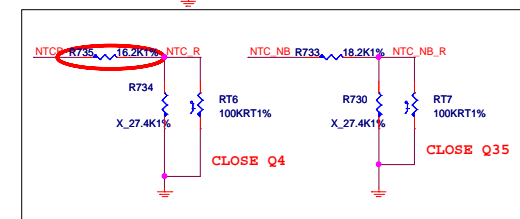
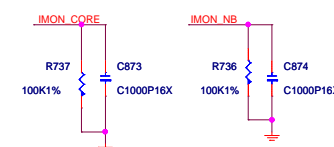
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs



$$5000\text{mA} \cdot 4 \cdot 1 + 1800 \cdot 2 = 23.6\text{A} < 26\text{A} \quad (7.68)$$



ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	18	2.2	1.3	10
RL (KOhm)	10	1.3	13	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



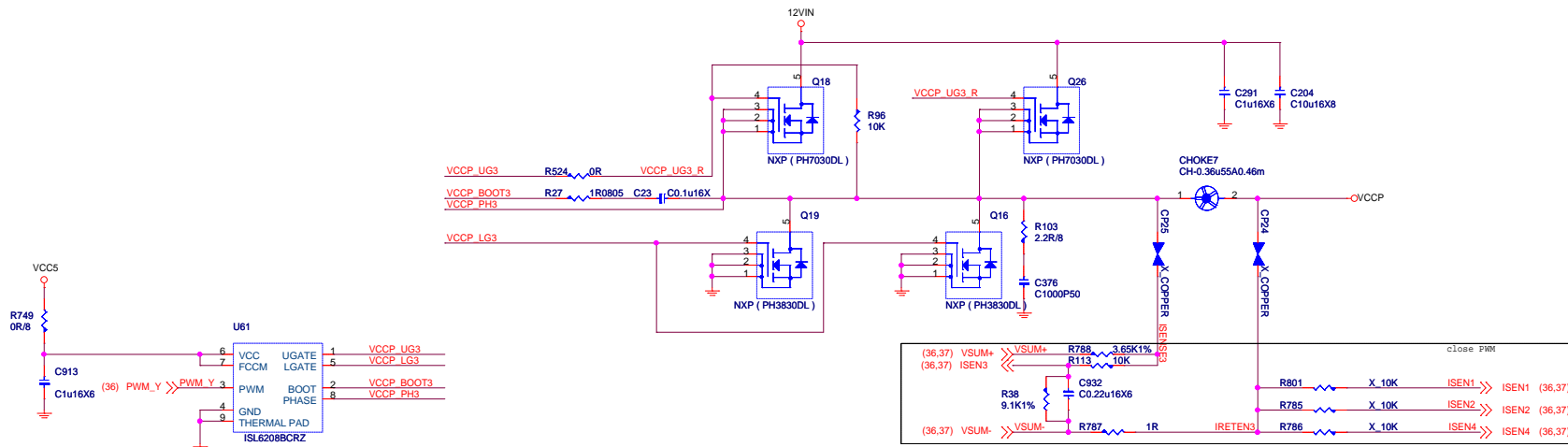
```
Power soulation
R523 -> 909 ohm (OCP)
R527 -> 539 ohm (OCP_NB)
R546 -> 5.23K ohm (NB_loadline)
```


2

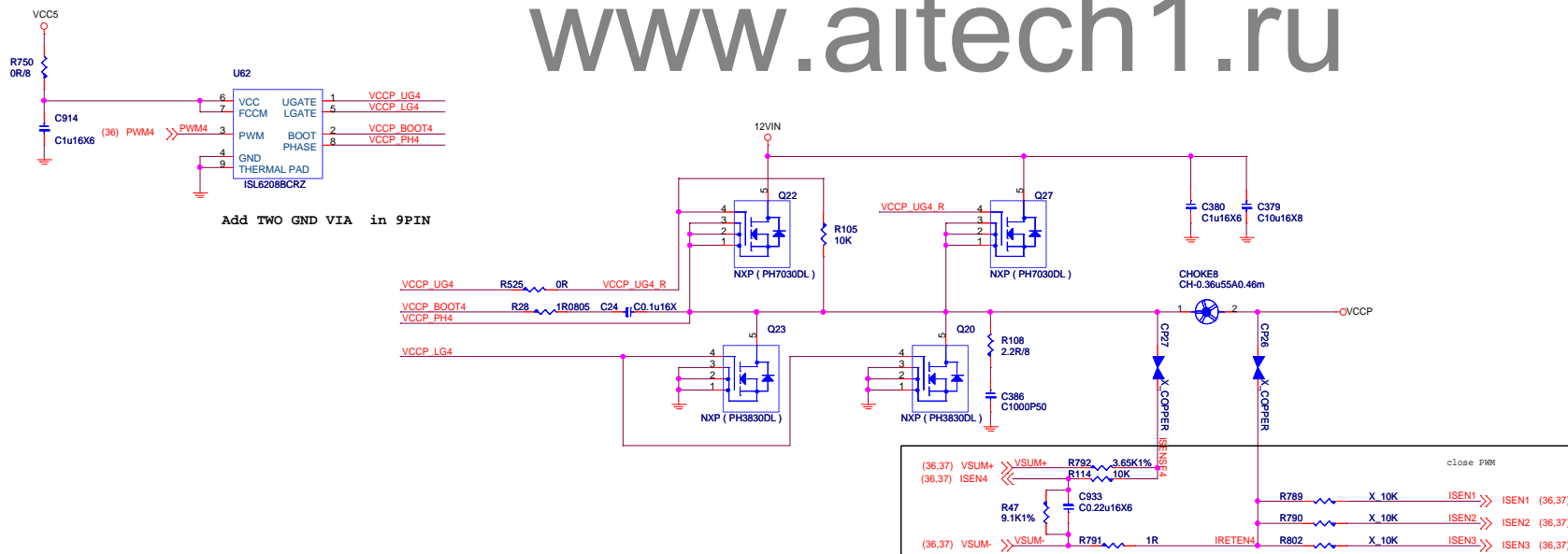


3





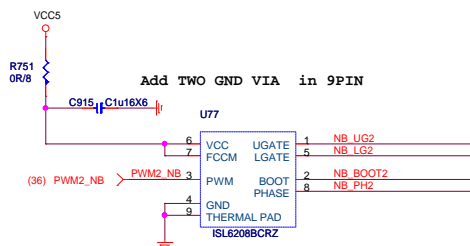
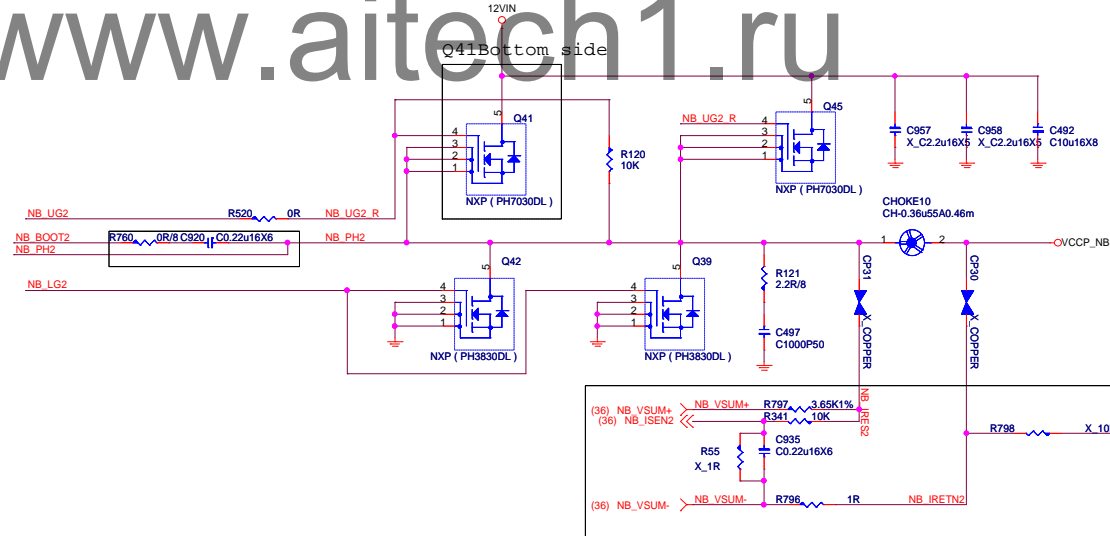
Add TWO GND VIA in 9PIN



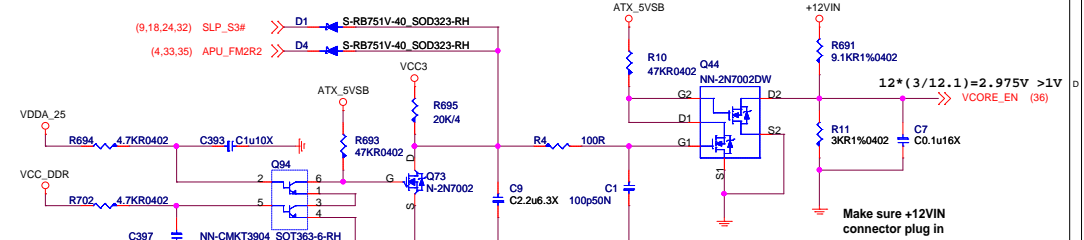
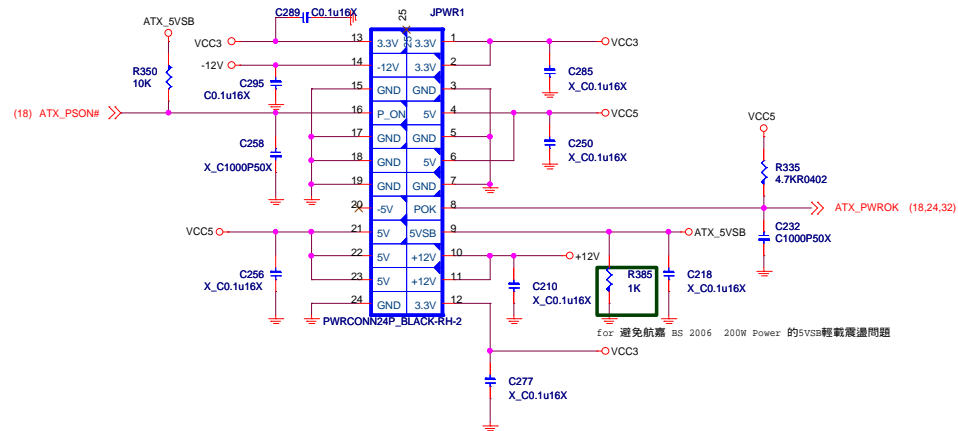
Add TWO GND VIA in 9PIN

www.aitech1.ru

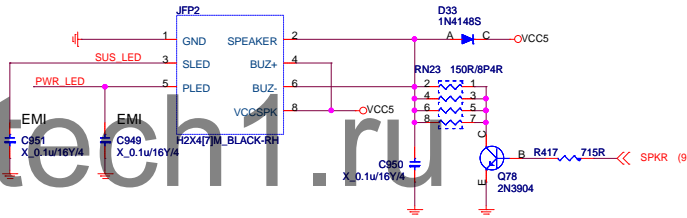
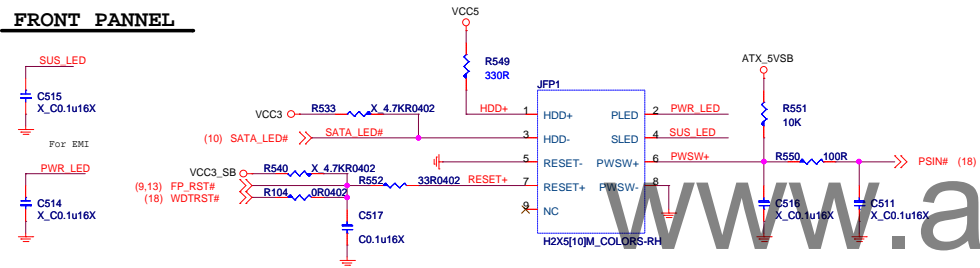
www.aitech1.ru



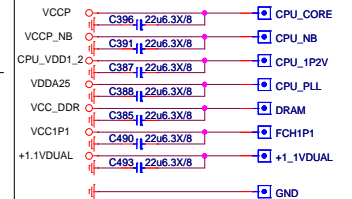
ATX CONNECTOR



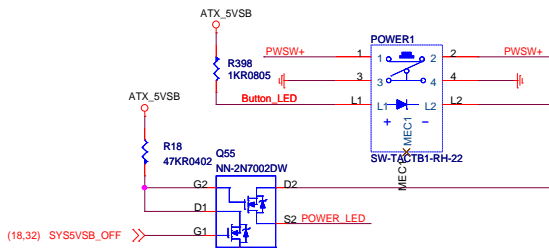
FRONT PANNEL



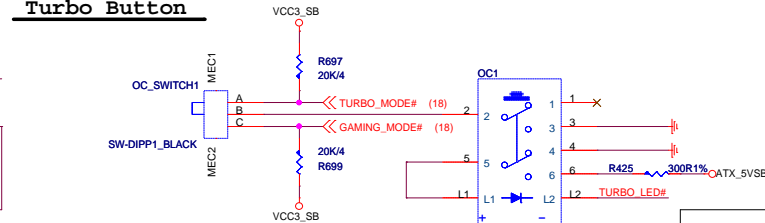
電壓測點



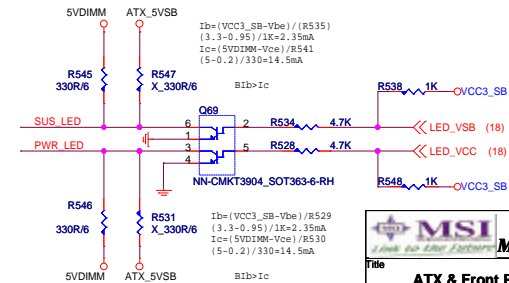
Power ON & Reset Button



Turbo Button



LED (for Fintek 71878)

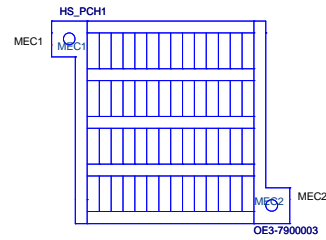
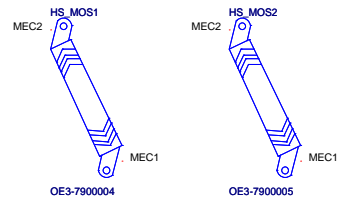


Add for EMI

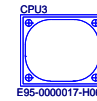
(29,31) DP_HPD >> C707 X C0.1u16X
(8,11,19) LPCCLK0_TPM >> C709 X C18p50N0402
VCC3 >> C710 X C0.1u16X
VCC3 >> C711 X C0.1u16X
VCC3 >> C713 X C0.1u16X
VCC3 >> C719 X C0.1u16X
VCC3 >> C745 X C0.1u16X
VCC3 >> C746 X C0.1u16X
VCC3 >> C748 X C0.1u16X
VCC3 >> C751 X C0.1u16X
VCC3 >> C730 X C0.1u16X
VCC3 >> C756 X C0.1u16X
VCC5 >> C715 X C0.1u16X
VCC5 >> C717 X C0.1u16X
VCC5 >> C718 X C0.1u16X
VCC5 >> C720 X C0.1u16X
VCC5 >> C727 X C0.1u16X
VCC5 >> C734 X C0.1u16X
VCC5 >> C731 X C0.1u16X
VCC5 >> C732 X C0.1u16X
VCC5 >> C733 X C0.1u16X
VCC5 >> C743 X C0.1u16X
VCC5 >> C744 X C0.1u16X
VCC5 >> C747 X C0.1u16X
VCCP >> C721 X C0.1u16X
VCCP >> C723 X C0.1u16X
VCCP >> C726 X C0.1u16X
VCCP >> C725 X C0.1u16X
VCCP >> C735 X C0.1u16X
VCCP >> C737 X C0.1u16X
VCCP >> C736 X C0.1u16X
VCCP >> C742 X C0.1u16X
VCCP >> C741 X C0.1u16X
VCC1P1 >> C738 X C0.1u16X
VCC1P1 >> C739 X C0.1u16X
VCC1P1 >> C740 X C0.1u16X

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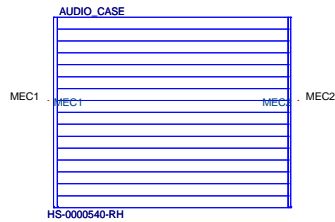
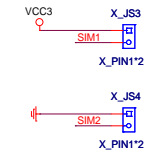
HEAT SINK



CPU Socket



Simulation



MANUAL PART



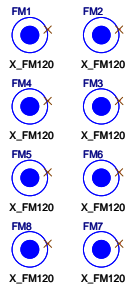
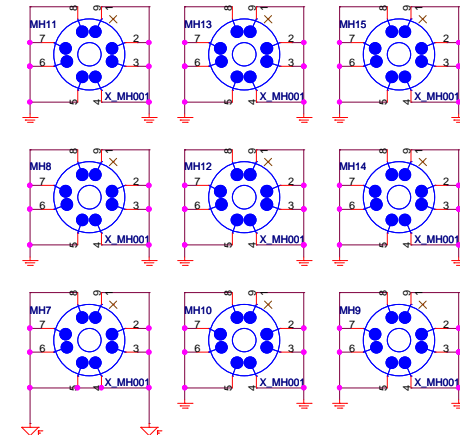
AVL:
D06-0100161-P52
D06-0100101-K26




7900-10
P00-079000A-G37, 精成, 23, 廣安恩斯通廠 (MSIS)
P00-079000A-E48, 競華, 23, 廣安恩斯通廠 (MSIS)

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Heat Sink hold



Optics Orientation Holes

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